

Mälardalen University Licentiate Thesis  
No.???

Static Timing Analysis of  
Parallel Software Using  
Abstract Execution  
– DRAFT –

Andreas Gustavsson

month year



**MÄLARDALEN UNIVERSITY**

School of Innovation, Design and Engineering  
Mälardalen University  
Västerås, Sweden

Copyright © Andreas Gustavsson, year  
ISSN ???-???  
ISBN ??-????-?-?  
Printed by Arkitektkopia, Västerås, Sweden  
Distribution: Mälardalen University Press

# Abstract

The Power Wall has stopped the past trend of increasing processor throughput by increasing the clock frequency and the instruction level parallelism. Therefore, the current trend in computer hardware design is to expose explicit parallelism to the software level. This is most often done using multiple processing cores situated on a single processor chip. The cores usually share some resources on the chip, such as some level of cache memory (which means that they also share the interconnect, e.g., a bus, to that memory and also all higher levels of memory), and to fully exploit this type of parallel processor chip, programs running on it will have to be parallel as well. Since multi-core processors are the new standard, even embedded real-time systems will (and some already do) incorporate this kind of processor and parallel code.

A real-time system is any system whose correctness is dependent both on its functional and temporal output. For some real-time systems, a failure to meet the temporal requirements can have catastrophic consequences. Therefore, it is of utmost importance that methods to analyze and derive safe estimations on the timing properties of parallel computer systems are developed.

This thesis presents an analysis that derives safe (lower and upper) bounds on the execution time of a given parallel program. The interface to the analysis is a rudimentary parallel programming language that is formally (both syntactically and semantically) defined in the thesis. The analysis is based on abstract execution, which is itself based on abstract interpretation techniques that have been commonly used within the field of timing analysis of single-core computer systems, to derive safe timing bounds in an efficient (although, over-approximative) way. Basically, abstract execution simulates the execution of several real executions of the analyzed program in one go.

The thesis proves the soundness of the presented analysis (i.e., that the estimated timing bounds are indeed safe) and also includes three case studies, each showing an important feature or characteristic of the analysis.



# Acknowledgment

Thanks!

Andreas Gustavsson  
Västerås, January 1, 2004 ??????????????



# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
1.1	Real-Time Systems . . . . .	1
1.2	Timing Analysis of Real-Time Systems . . . . .	3
1.3	Research Questions . . . . .	5
1.4	Pilot Study . . . . .	5
1.5	Approach . . . . .	6
1.6	Contribution . . . . .	7
1.7	Included Publications . . . . .	8
1.8	Thesis Outline . . . . .	9
<b>2</b>	<b>Related Work</b>	<b>11</b>
2.1	Static Timing Analysis . . . . .	11
2.2	Multi-Core Analyzability . . . . .	13
<b>3</b>	<b>Preliminaries</b>	<b>15</b>
3.1	Partially Ordered Sets & Complete Lattices . . . . .	15
3.2	Constructing Complete Lattices . . . . .	18
3.3	Galois Connections & Galois Insertions . . . . .	20
3.4	Constructing Galois Connections . . . . .	23
3.5	Constructing Galois Insertions . . . . .	31
3.6	The Interval Domain . . . . .	33
<b>4</b>	<b>PPL: A Parallel Programming Language</b>	<b>37</b>
4.1	States & Configurations . . . . .	38
4.2	Semantics . . . . .	40
4.3	Collecting Semantics . . . . .	52

<b>5</b>	<b>Abstractly Interpreting PPL</b>	<b>53</b>
5.1	Arithmetical Operators for Intervals . . . . .	54
5.2	Abstract Register States . . . . .	54
5.3	Abstract Evaluation of Arithmetical Expressions . . . . .	56
5.4	Boolean Restriction . . . . .	57
5.5	Abstract Variable States . . . . .	58
5.6	Abstract Lock States . . . . .	74
5.7	Abstract Configurations . . . . .	78
5.8	Abstract Semantics . . . . .	85
<b>6</b>	<b>Safe Timing Analysis by Abstract Execution</b>	<b>137</b>
6.1	Abstract Execution . . . . .	137
6.2	Timing Analysis . . . . .	158
<b>7</b>	<b>Examples</b>	<b>161</b>
7.1	Communication . . . . .	161
7.2	Synchronization – Deadlocks . . . . .	166
7.3	Synchronization – Deadline Miss . . . . .	169
<b>8</b>	<b>Conclusions</b>	<b>171</b>
8.1	The Underlying Architecture . . . . .	171
8.2	Algorithmic Structure & Complexity . . . . .	172
8.3	Non-terminating Transition Sequences . . . . .	175
8.4	The Research Questions . . . . .	176
8.5	Other Applications of the Analysis . . . . .	177
8.6	Future Work . . . . .	178
	<b>Bibliography</b>	<b>179</b>
<b>A</b>	<b>Notation &amp; Nomenclature</b>	<b>189</b>
<b>B</b>	<b>List of Assumptions</b>	<b>193</b>
<b>C</b>	<b>List of Definitions</b>	<b>195</b>
<b>D</b>	<b>List of Figures</b>	<b>197</b>
<b>E</b>	<b>List of Tables</b>	<b>199</b>
<b>F</b>	<b>List of Algorithms</b>	<b>201</b>



<b>G List of Lemmas</b>	<b>203</b>
<b>H List of Theorems</b>	<b>205</b>
<b>Index</b>	<b>207</b>



# Chapter 1

## Introduction

This chapter starts by introducing the fundamental concepts used within the field of the thesis. It also states the asked research questions, the approach used to answer the questions and the resulting contributions of the thesis. This chapter also presents the papers included in the thesis and a pilot study on using model-checking for timing analysis of parallel real-time systems.

### 1.1 Real-Time Systems

As computers have become smaller, faster, cheaper and more reliable, their range of use has rapidly increased. Today, everything from wrist watches to airplanes are computer-controlled. These types of systems are commonly referred to as *embedded* systems; i.e., one or more controller chips with accompanying software are embedded within the product. It has been approximated that over 99 percent of the worldwide production of computer chips are destined for embedded systems [9].

A *real-time* system is often an embedded system for which the timing behavior is of great importance. More formally, the Oxford Dictionary of Computing gives the following definition of a real-time system [40].

“Any system in which the time at which output is produced is significant. This is usually because the input corresponds to some movement in the physical world, and the output has to relate to that same movement. The lag from input time to output time must be sufficiently small for acceptable timeliness.”

The word “timeliness” refers to the total system and can be dependent on mechanical properties like inertia. One example is the compensation of temporary deviations in the supporting structure (e.g., a twisting frame) when firing a missile to keep the missile’s exit path constant throughout the process. Another example is to fire the airbag in a colliding car. This should not be done too soon, or the airbag will have lost too much pressure upon the human impact, and not too late, or the airbag could cause additional damage upon impact; i.e., the inertia of the human body and the retardation of the colliding car both impact on the timeliness of the airbag system. It should thus be apparent that the correctness of a real-time system depends both on the logical result of the performed computations and the time at which the result is produced.

Real-time systems can be divided into two categories: hard and soft real-time systems. Hard real-time systems are such that failure to produce the computational result within certain timing bounds could have catastrophic consequences. One example of a hard real-time system is the above-mentioned airbag system. Soft real-time systems, on the other hand, can tolerate missing these deadlines to some extent and still function properly. One example of a soft real-time system is a video displaying device. Missing to display a video frame within the given bounds will not be catastrophic (but perhaps annoying to the viewer if it occurs too often). The video will still continue to play (although, perhaps with reduced displaying quality), assuming that the system is not overloaded in general.

The current trend in computer hardware design is to make parallelism explicitly available to the programmer, often in the form of multiple processing cores on the same chip. This strategy helps increasing the chip’s throughput without hitting the power wall since the individual processing cores on the multi-core chip are usually simpler than a single core implemented on the equivalent chip area [70]. The cores typically share some resources, such as some level of on-chip cache memory, which introduces dependencies and conflicts between the cores; e.g., simultaneous accesses from two or more cores to shared resources will introduce delays for some of the cores. Processor chips of this kind of *multi-core* architecture are currently being used in real-time systems within, for example, the automotive industry.

To fully utilize the multi-core architecture, algorithms will have to be parallelized over multiple tasks (e.g., threads). This means that the tasks will have to share resources and communicate and synchronize with each other. There already exist software libraries for explicitly parallelizing sequential code automatically. One example of such a library available for C/C++ and Fortran code running on shared-memory machines is OpenMP [64]. The conclusion is that

parallel software running on parallel hardware is already available today and will probably be the standard way of computing in the future, also for real-time systems.

When proving the correctness of, and/or the schedulability of the tasks in, a real-time system, it is, as far as the author knows, always assumed that *safe* (i.e., not under-approximated) bounds on the timing behavior of all tasks in the system are known. The timing bounds are, for example, used as input to algorithms that prove or falsify the schedulability of the tasks in the system [4, 22, 54]. Therefore, it is of crucial importance that methods for deriving safe timing bounds (referred to as estimates) for this type of parallel computational systems are defined.

This thesis presents a method that derives safe estimates on the timing bounds for the described type of systems. The method mainly targets hard real-time systems. However, it can be applied to any computer system fitting the assumptions made in the upcoming chapters.

## 1.2 Timing Analysis of Real-Time Systems

A program's execution time (i.e., the amount of time it takes to execute the entire program from its entry point to its exit point) is not constant; it is dependent on the initial system state. This state includes the input to the program (i.e., the values of its arguments), the hardware state (e.g., cache memory contents) and the state of any other software that is executing on the same hardware. However, for any program and any set of initial states, at least one of the resulting execution times will be equal to the shortest execution time for the given program and set of initial states. The shortest execution time is referred to as the Best-Case Execution Time (*BCET*). Likewise, at least one of the resulting execution times will be equal to the longest execution time for the given program and set of initial states. The longest execution time is referred to as the Worst-Case Execution Time (*WCET*).

Traditionally, when computers were purely sequential, the main focus of timing analysis only targeted estimations of the *WCET*. This was possible because the analyzed systems did not suffer from any timing anomalies, which meant that the local worst-case scenario (i.e., the longest possible execution time for a single instruction, or a block of instructions) always resulted in the global worst-case. However, when introducing multi-core architectures with shared memory, this is no longer the case [1, 56, 76]. This means that the only safe option is to take all the possible execution times between, and including,

the local BCET and WCET into account when deriving the global (BCET and) WCET.

Today, there exist several algorithms and tools that strive to derive a *safe* and *tight* (i.e., not too over-approximate) estimate of the WCET of a sequential task targeted for sequential hardware. Some examples of such tools are aiT [20, 91], Bound-T [37, 91], Chronos [49, 91], Heptane [91], OTAWA [6], RapiTime [75, 91], SWEET [17, 91], SymTA/P [91] and TuBound [72, 91]. aiT, Bound-T and RapiTime are commercial tools while the others are primarily research prototypes. aiT, Bound-T, Chronos, Heptane, OTAWA and TuBound are purely static tools while SWEET and SymTA/P mainly use static WCET analysis techniques, but also dynamic techniques to some extent. RapiTime is heavily based on dynamic techniques.

In *dynamic* WCET analysis, measurements of the actual execution time of the software running on the target hardware are performed. This method is not guaranteed to execute the program's worst-case path, though, which could, for example, include some error-handling routine that is only rarely executed. Thus, the WCET might be gravely under-estimated; i.e., there might exist paths through the code with considerably worse (longer) execution times than the worst execution time detected by the measurements.

In *static* WCET analysis, the program code and the properties of the target hardware are analyzed without actually executing the program. Instead, the analysis is based on the semantics of the programming language constructs used to define the program and a (timing) model of the target hardware. Static methods usually try to find a tight estimation of the WCET, but always safely over-estimate it.

Static WCET analyses are normally split into three subtasks: the *low-level analysis*, which attempts to find safe timing estimates for executions of code sequences, the *flow analysis*, which constrains the possible paths through the code, and the *calculation*, where the most time-consuming path is found, using information derived in the first two phases. This traditional approach assumes that the analyzed program consists of a single flow of control; i.e., is sequential. In a parallel program, there are several flows of control, possibly with dependencies among them. The consequence is that the traditional three-phase approach is not directly applicable when analyzing arbitrary parallel programs executing on parallel shared-memory architectures.

This thesis presents a static method that derives safe estimations of the BCET and WCET of a parallel program by combining the three phases into one single phase; i.e., the method directly calculates the timing bound estimates while analyzing the semantic behavior of the program, based on a (safe) timing

model of the underlying architecture.

Note that solving the problem of finding the actual WCET in the general case is comparable to solving the halting-problem (i.e., determining whether the program will terminate), which is an undecidable problem (c.f., [45]). Thus, the space of possible system states that a WCET analysis must search through could be extremely large, or even infinite, in the general case. This means that the analysis itself might not terminate in the general case. Therefore, techniques to increase the probability of, or even more desirable, guarantee, analysis termination must be derived. For many of the traditional methods for analyzing sequential programs, there are ways to guarantee termination using widening/narrowing techniques [62]. These techniques are not directly applicable to the method presented in this thesis, though.

### 1.3 Research Questions

This thesis mainly tries to answer the following questions.

**Question 1:** *“What are the distinguishing features of a parallel computer system (i.e., the hardware and software combination) that must be taken into account in a timing analysis on the code level?”*

**Question 2:** *“How can a parallel computer system be analyzed to derive safe and tight estimations on its timing bounds?”*

**Question 3:** *“How can analysis termination be guaranteed?”*

### 1.4 Pilot Study

Model-checking is a technique for verifying properties of a model of some system. The idea of using model-checking to perform WCET analysis has been investigated and shown to be adequate for analyzing parts of a single-core system [38, 60].

Timed automata<sup>1</sup> can be used to model real-time systems [3]. An automaton can be viewed as a state machine with locations and edges [43]. A state represents certain values of the variables in the system and which location of an automaton is active, while the edges represent the possible transitions from one state to another [43]. (Continuous) time is expressed as a set of real-valued

---

<sup>1</sup>The formal syntax and semantics of timed automata can be found in [2] and [43].

variables called clocks. UPPAAL<sup>2</sup> [7, 47, 89] is a tool used to model, simulate and verify networks of timed automata [7, 8, 43].

Preceding the work presented in this thesis, an initial study [30] in which UPPAAL was used to model, and derive high precision estimates on the timing bounds of, a small parallel real-time system was performed. The paper shows that timing analysis of parallel real-time systems can be performed using the model-checking techniques available in for example UPPAAL. However, the proposed method (i.e., the way the system was modeled and analyzed) did not scale very well, for example with respect to the number of threads in the analyzed program. Therefore, it was decided not to continue on the pure model-checking path (although, there might be other ways to model the system that would succeed better).

## 1.5 Approach

The approach used in this thesis is to statically calculate safe BCET and WCET estimations by abstractly executing the analyzed program (c.f., [23, 28]) using a safe timing model of the underlying hardware. As previously discussed, statically computing the exact set of possible semantic states for an arbitrary program is an extremely complex task. Using abstract execution (which is based on abstract interpretation techniques), at least all the possible semantic states, given some set of initial system states, are considered, but in a less complex way.

Abstract interpretation [14, 23, 62] is a method for safely approximating the program semantics and can be used to obtain a set of possible abstract states for each point in a program. An abstract state collects, and most often over-approximates, the information given by a set of concrete semantic states. This means that an analysis based on abstractly interpreting the semantics of a program can become less complex and more efficient, but might suffer from imprecision, compared to an analysis based on the concrete semantics.

The concrete semantics of an arbitrary programming language can be abstracted in many different ways. The choice of abstraction is done by defining an abstract domain. An abstract domain is essentially the set of all possible abstract states that fit the definition of the domain.

An example of an abstract domain is **Intv**, defined as  $\{[z_1, z_2] \mid -\infty \leq z_1 \leq z_2 \leq \infty \wedge z_1, z_2 \in \mathbb{Z} \cup \{-\infty, \infty\}\}$ ; i.e., the set of all intervals that “fit inside”

---

<sup>2</sup>An introduction to UPPAAL and the formal semantics of networks of timed automata are given in [7] and [43], respectively.



$[-\infty, \infty]$ . (Note that the domain **Intv** is completely defined in Section 3.6.) This domain can be used to over-approximate the concrete domain  $\{z \in \mathbb{Z} \cup \{-\infty, \infty\} \mid -\infty \leq z \leq \infty\} = \mathbb{Z} \cup \{-\infty, \infty\}$ ; i.e., the set of all integers between (and including)  $-\infty$  and  $\infty$ .

Assume that the program variable  $x$  can have the value  $v$ , such that  $v \in \{1, 2, 5, 8\}$ , in a given point of the program according to the concrete semantics (i.e.,  $x$  has four possible values in the given program point). In the abstract domain, the value of  $x$  could safely be represented by  $[1, 8]$ . This is an over-approximation since turning the abstract value into a set of concrete values yields  $[1, 8] \rightarrow \{1, 2, 3, 4, 5, 6, 7, 8\} \supseteq \{1, 2, 5, 8\}$ . It can be noted that  $[1, 8]$  is the best (tightest) approximation of the values of  $x$ , since  $[1, 8]$  is the smallest interval containing all the possible concrete values of  $x$ .

Abstract execution is simply a way to abstractly simulate the execution of the analyzed program. This is done by collecting several concrete states into one (or, for some situations, several) abstract states using abstract interpretation, as discussed above. The existence of a timing model (of the underlying architecture) that provides safe information on the timing properties of individual operations within the analyzed program when executed in a particular system state allows the BCET and WCET of the analyzed program to be safely estimated.

Basically, the only assumption made on the underlying architecture is that it provides (or can simulate) a shared memory address space, that can be used for communication, and shared resources, that can be used for synchronization. One example of such an architecture is a multi-core CPU. Another example is a virtualization environment that runs on top of a distributed system and provides a shared memory view. Yet another example is any real-time operating system; e.g., VxWorks [92].

## 1.6 Contribution

The main contributions of this thesis are the following.

1. PPL: a formally defined, rudimentary, parallel programming language for real-time systems. The semantics of PPL includes timing behavior and is defined based on the familiar notation of operational semantics (c.f., [63]).
2. An abstraction of the PPL semantics where concrete points in time are abstracted using intervals.

3. A *safe* timing analysis based on the abstract semantics of PPL. A complete correctness/soundness proof is provided.

## 1.7 Included Publications

This thesis includes the material presented in the following papers. Andreas Gustavsson is the main author of all the listed publications and has alone contributed with all the technical material presented in them.

### Paper A

*Worst-Case Execution Time Analysis of Parallel Systems*

Andreas Gustavsson.

Presented at the RTiS workshop, 2011.

This Paper addresses contribution 1 and presents the first definition of the parallel programming language and a very simple (non-generalized) hardware timing model.

### Paper B

*Toward Static Timing Analysis of Parallel Software*

Andreas Gustavsson, Jan Gustafsson and Björn Lisper.

Presented at the WCET workshop, 2012.

This Paper addresses contributions 2 and 3 and presents a work-in-progress timing analysis that can analyze all aspects of a parallel program, except synchronization. The presented analysis uses abstract execution to derive safe estimations of the BCET and WCET of the analyzed program.

### Paper C

*Toward Static Timing Analysis of Parallel Software - Technical Report*

Andreas Gustavsson, Jan Gustafsson and Björn Lisper.

Technical report, 2012.

This Paper addresses contributions 2 and 3 and is an extended version of Paper B. The Paper includes all the mathematical details and a sketch for the correctness/soundness proof.

**Paper D***Timing Analysis of Parallel Software Using Abstract Execution*

Andreas Gustavsson, Jan Gustafsson and Björn Lisper.

Submitted to the VMCAI conference, 2014.

This paper addresses contributions 1, 2 and 3 and summarizes the work presented in this thesis. It presents a timing analysis that is based on the analysis defined in Papers B and C. The presented analysis derives safe estimations of the BCET and WCET for any program defined using a slightly modified version of the language presented in Paper A (i.e., PPL), given some (safe) timing model of the underlying architecture.

**1.8 Thesis Outline**

The rest of this thesis is organized as follows.

**Chapter 2** presents some research that is closely related to the material presented in this thesis.

**Chapter 3** introduces the reader to the fundamental concepts and theories needed to understand the contents of the following chapters.

**Chapter 4** formally defines PPL, a parallel programming language.

**Chapter 5** presents a semi-safe abstraction of the PPL semantics. Note that the abstraction is not safe for arbitrary PPL programs and that special care must be taken if using it (c.f., Chapter 6).

**Chapter 6** defines a *safe* timing analysis using abstract execution based on the abstraction made in Chapter 5.

**Chapter 7** presents some examples that show how the analysis presented in Chapter 6 handles communication and synchronization in PPL programs.

**Chapter 8** discusses the research questions and the analysis presented in Chapter 6. The chapter also gives pointers to future work.

For the reader's convenience, the following appendices are provided.

**Appendix A** summarizes the notations and nomenclature used in this thesis.

**Appendices B-H** present listings of the assumptions, definitions, figures, tables, algorithms, lemmas and theorems defined in this thesis, respectively.

## Chapter 2

# Related Work

WCET-related research started with the introduction of timing schemas by Shaw in 1989 [82]. Shaw presents rules to collapse the CFG (Control Flow Graph) of a program until a final single value represents the WCET. Excellent overviews of the WCET research from the years 2000 and 2008 can be found in [73] and [91] respectively. The field of WCET analysis for parallel systems is quite new, so there is no solid foundation of previous research to stand on.

### 2.1 Static Timing Analysis

The field of static WCET analysis has, just until recently, mainly been focusing on single-processor systems. In the field of low-level analysis, most research efforts have been dedicated to analyzing the effects of different hardware features, including pipelines [16, 35, 52, 83, 88], caches [50, 52, 88, 90], branch predictors [13], and super-scalar CPUs [51, 80].

Within flow analysis, most research has been dedicated to *loop bound* analysis. Flow analysis can also identify *infeasible paths*, i.e., paths which are executable according to the program control-flow graph structure, but not feasible when considering the semantics of the program and possible input data values. There are a number of approaches to flow analysis, using e.g., abstract interpretation, symbolic execution, Presburger arithmetics, specialized data flow analyses, and syntactical analysis of parse trees [28, 36, 37, 55, 88].

There is also some research on data flow analysis for parallel programs [15, 21, 46], which is of relevance to WCET analysis. Constant propagation

has also been considered [48]. A survey of analyses for concurrent and parallel programs is found in [77].

Three main methods exist for the WCET calculation: The tree-based method [12, 13, 52], originating from Park's *timing schemas* [68]; the *path-based* method [35, 84]; and the *Implicit Path Enumeration Technique* (IPET) [17, 37, 50, 74, 88], where the WCET calculation problem is formulated as an Integer Linear Programming (ILP) problem, and the set of execution paths is restricted by linear constraints.

An alternative way of computing the ILP problem is by using a graph-based approach [74]. A comparison of the graph-based and IPET approaches is performed in [38]. The graph-based approach is conducted using model-checking in UPPAAL [7, 47, 89]. It is shown that IPET outperforms the model-checking-based approach, but that model-checking allows for calculating tight WCET bounds and easy integration of complex hardware models. A combined approach is proposed, where model-checking is used to analyze local regions of the code, while IPET is used to solve the global analysis. Another motivation to why model-checking could be useful in WCET analysis can be found in [60].

For analyses based on abstract execution, it is possible to calculate the BCET and WCET estimates of sequential programs during the abstract execution, without first generating flow facts [18, 28]. This thesis uses basically the same approach, but applies it to explicitly parallel programs.

Some research has been conducted within the field of static WCET analysis for multi-core and other types of multi-processor systems. A static method for analyzing multi-core processors with a shared L2 instruction cache has been presented [94]. A limitation of this analysis is that the L1 data cache is assumed to be perfect (i.e., all accesses are assumed to be hits, which is generally not the case) and thus does not affect the contents of the L2 cache. Based on this work, the same authors also address the same problem for the case that the shared L2 cache is direct-mapped [95].

There is also an approach for analyzing multi-cores with a shared L2 instruction cache (that still assumes a perfect L1 data cache) that takes effects from timing anomaly influenced pipelines into account [11].

Staschulat et al. [85] consider an integrated task- and system-level analysis to estimate memory access times for sequential tasks running in parallel with tasks executing on other processors. Their approach requires full information about all tasks running in the system, and it makes quite strong assumptions about the task model.

Mittermayr and Blieberger [61] use a graph based approach and Kronecker algebra to calculate an estimation of the WCET of a concurrent program. The

graph is referred to as CPG (Concurrent Program Graph) and plays a role similar to the CFG for sequential programs.

Potop-Butucaru and Puaut [71] target static timing analysis of parallel processors where “channels” are used to communicate between, and synchronize, the parallel tasks. Additional edges representing such communication and synchronization are then used to connect the CFGs of the individual tasks. The goal of this approach is to enable the use of the traditional three-phase analysis when analyzing parallel systems.

Ozaktas et al. [65] focus on analyzing synchronization delays experienced by tasks executing on time-predictable shared-memory multi-core architectures.

Lv et al. [57] and Wu and Zhang [93] use model-checking of timed automata to perform WCET analysis. In this approach, a timed automata-model of the system to be analyzed is created. Then, specific properties of the model are verified to find a WCET estimate for the analyzed system. The achievable tightness of the WCET estimate depends on the level of details in the timed automata-model.

Both papers mainly propose methods for reducing the size of the state space by altering the program model without affecting the true WCET of the model. This is a very important aspect when using model-checking overall. If the model is too large and complex, the state space will “explode”, which means that the number of possible states is very large and analyzing the model becomes infeasible.

Lv et al. [58] have also combined abstract interpretation with model-checking to avoid the scalability problems found in, e.g., [30]. This work does not focus on explicitly parallel software, though.

## 2.2 Multi-Core Analyzability

Some other research addresses the problem of (low) predictability in multi-core processors. This work mostly gives multi-core design guidelines and suggestions on how to use additional or modified hardware to increase the predictability, and thus, the analyzability. In an extension to the method found in [94], memory bits for each instruction is used to determine whether the instruction should be cached or not [34]. E.g., to avoid pollution of the shared cache, “Static Single Usage” instructions (i.e., instructions in the program that are only referenced/executed once) should not be cached. This generates the possibility to determine a tighter WCET estimate.

Arbiters (hardware circuits) can be added to a shared memory multi-core processor to synchronize the memory accesses from different cores in order to increase the timing predictability of the system [66]. The result is a multi-core architecture that can be analyzed with existing single-core (and single-task) WCET analysis tools.

GAMC [67] is an SDRAM controller which upper bounds the delay a core can suffer from memory-access interferences from other cores. This is an important approach since the largest memory access latency will occur when accessing the main memory. The result is tight WCET approximations which only differ a few percent from the largest measured execution times, for a specific analyzed program suite.

Time Division Multiple Access (TDMA)-based memory bus access policies can also be introduced to make all memory accesses predictable, regarding the WCET [4, 79]. The problem with this approach is that the performance of the processor will be seriously degraded since, in the average case, a memory access from any core will be stalled for half the TDMA period (and the whole period in the worst case).

Kelter et al. [44] suggest to use the Priority Division (PD) protocol instead of the TDMA protocol. They show that PD is a very promising replacement for TDMA that provides predictability while not degrading the performance as severely as TDMA.

The MERASA project [59, 78] strives towards providing a timing analyzable multi-core CPU with a system level software (c.f., operating system). A case study [78] has been performed, in which an estimation of the WCET of a parallel 3D multi-grid solver, executing on the MERASA multi-core platform, is derived. The parMERASA project [69] is a continuation of the MERASA project.



## Chapter 3

# Preliminaries

In general, basing a timing analysis on the concrete semantics of a program is infeasible due to the enormous number of states that must be explored. As discussed in Section 1.5, abstract interpretation [14, 23, 62] is a method for *safely* approximating the concrete program semantics and can be used to obtain a set of possible abstract states for each point in a program. An abstract state collects, and most often over-approximates, the information given by a *set* of concrete semantic states. This means that an analysis based on abstractly interpreting the semantics of a program can become less complex and more efficient compared to an analysis based on the concrete semantics. The analysis presented in this thesis is based on abstract interpretation. Therefore, this chapter introduces the foundations used by abstract interpretation techniques.

NOTE. A summary of the notation and nomenclature used in this thesis can be found in Appendix A.

### 3.1 Partially Ordered Sets & Complete Lattices<sup>1</sup>

The *relation*, as described by  $\mathcal{R}: A \times B \rightarrow \{\text{true}, \text{false}\}$  where  $A \times B$  is the Cartesian product of the two sets  $A$  and  $B$ , between two elements  $a \in A$  and

---

<sup>1</sup>Extensive introductions to complete lattices can be found in many textbooks, e.g., [62].

$b \in B$  is denoted by  $a \mathcal{R} b$ . Given that for every  $a \in A$ , there is at most one element,  $b \in B$ , such that  $a \mathcal{R} b$ , then  $\mathcal{R}$  is said to be a *partial function* from  $A$  to  $B$ . Given that for every  $a \in A$ , there is exactly one element,  $b \in B$ , such that  $a \mathcal{R} b$ , then  $\mathcal{R}$  is said to be a *total function* from  $A$  to  $B$ .

A *partial ordering* is a relation  $\sqsubseteq: A \times A \rightarrow \{\text{true}, \text{false}\}$  that is reflexive (i.e.,  $\forall a \in A : a \sqsubseteq a$ ), transitive (i.e.,  $\forall a, a', a'' \in A : ((a \sqsubseteq a' \wedge a' \sqsubseteq a'') \Rightarrow a \sqsubseteq a'')$ ) and anti-symmetric (i.e.,  $\forall a, a' \in A : ((a \sqsubseteq a' \wedge a' \sqsubseteq a) \Rightarrow a = a')$ ). The pair  $(A, \mathcal{R})$  is a *partially ordered set* if  $\mathcal{R}: A \times A \rightarrow \{\text{true}, \text{false}\}$  is a partial ordering on  $A$ .

A subset  $A'$  of  $A$  has  $a \in A$  as an *upper bound* if  $\forall d' \in A' : d' \sqsubseteq a$  and as a *lower bound* if  $\forall d' \in A' : a \sqsubseteq d'$ . The element  $a \in A$  is the *least upper bound* of  $A'$  if  $a$  is an upper bound of  $A'$  and for all other upper bounds,  $a' \in A$ , of  $A'$ ,  $a \sqsubseteq a'$  (c.f., Definition 3.28). The element  $a \in A$  is the *greatest lower bound* of  $A'$  if  $a$  is a lower bound of  $A'$  and for all other lower bounds,  $a' \in A$ , of  $A'$ ,  $a' \sqsubseteq a$  (c.f., Definition 3.27). Note that a greatest lower bound and/or a least upper bound might not exist for all subsets of a partially ordered set. When they do exist, they are unique (since  $\sqsubseteq$  is anti-symmetric) and will be denoted  $\sqcap A'$  and  $\sqcup A'$ , respectively. The shorthand  $a \sqcap a'$  will be used to denote  $\sqcap \{a, a'\}$ . Likewise,  $a \sqcup a'$  will be used to denote  $\sqcup \{a, a'\}$ .

A *complete lattice*,  $V = \langle V, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$ , is a partially ordered set,  $(V, \sqsubseteq)$ , such that all subsets have greatest lower bounds and least upper bounds. The least element of  $V$  is denoted  $\perp$  (the *bottom element*) and is defined as  $\perp = \sqcup \emptyset = \sqcap V$ . The greatest element of  $V$  is denoted  $\top$  (the *top element*) and is defined as  $\top = \sqcup V = \sqcap \emptyset$ .

The properties of *monotone*, *completely additive* and *completely multiplicative* functions are given in Definitions 3.1, 3.2 and 3.3, respectively. Note that when  $V_1$  and  $V_2$  are complete lattices, all subsets of these sets have least upper bounds and greatest lower bounds. Lemma 3.4 states some specific properties of a completely multiplicative function.

**Definition 3.1 (Monotone function):**

A function,  $f: V_1 \rightarrow V_2$ , between the partially ordered sets  $V_1 = (V_1, \sqsubseteq_1)$  and  $V_2 = (V_2, \sqsubseteq_2)$  is *monotone* if:

$$\forall v_1, v'_1 \in V_1 : v_1 \sqsubseteq_1 v'_1 \Rightarrow f(v_1) \sqsubseteq_2 f(v'_1) \quad \square$$

**Definition 3.2 (Completely additive function):**

A function,  $f: V_1 \rightarrow V_2$ , between the partially ordered sets  $V_1 = (V_1, \sqsubseteq_1)$  and  $V_2 = (V_2, \sqsubseteq_2)$  is *completely additive* if for all  $V'_1 \subseteq V_1$

$$f(\sqcup_1 V'_1) = \sqcup_2 \{f(v) \mid v \in V'_1\}$$

whenever  $\sqcup_1 V'_1$  and  $\sqcup_2 \{f(v) \mid v \in V'_1\}$  exist.  $\square$

**Definition 3.3 (Completely multiplicative function):**

A function,  $f : V_1 \rightarrow V_2$ , between the partially ordered sets  $V_1 = (V_1, \sqsubseteq_1)$  and  $V_2 = (V_2, \sqsubseteq_2)$  is completely multiplicative if for all  $V'_1 \subseteq V_1$

$$f(\sqcap_1 V'_1) = \sqcap_2 \{f(v) \mid v \in V'_1\}$$

whenever  $\sqcap_1 V'_1$  and  $\sqcap_2 \{f(v) \mid v \in V'_1\}$  exist.  $\square$

**Lemma 3.4 (Completely multiplicative functions):**

If  $V = \langle V, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$  and  $\tilde{V} = \langle \tilde{V}, \tilde{\sqsubseteq}, \tilde{\sqcup}, \tilde{\sqcap}, \tilde{\perp}, \tilde{\top} \rangle$  are complete lattices and  $\tilde{V}$  is finite, then the three conditions

1.  $\gamma : \tilde{V} \rightarrow V$  is monotone,
2.  $\gamma(\tilde{\top}) = \top$ , and
3.  $\gamma(\tilde{v} \tilde{\sqcap} \tilde{v}') = \gamma(\tilde{v}) \sqcap \gamma(\tilde{v}')$ , whenever  $\tilde{v} \tilde{\sqsubseteq} \tilde{v}' \wedge \tilde{v}' \tilde{\sqsubseteq} \tilde{v}$ , where  $\tilde{v}, \tilde{v}' \in \tilde{V}$

are jointly equivalent to  $\gamma : \tilde{V} \rightarrow V$  being completely multiplicative.  $\square$

PROOF (c.f., [62]). Assume that  $V = \langle V, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$  and  $\tilde{V} = \langle \tilde{V}, \tilde{\sqsubseteq}, \tilde{\sqcup}, \tilde{\sqcap}, \tilde{\perp}, \tilde{\top} \rangle$  are complete lattices and that  $\tilde{V}$  is finite.

First note that if  $\gamma : \tilde{V} \rightarrow V$  is completely multiplicative, then the three conditions trivially hold. Next, assuming that the three conditions are fulfilled, it will be proven that

$$\gamma(\tilde{\sqcap} \tilde{V}') = \sqcap \{\gamma(\tilde{v}) \mid \tilde{v} \in \tilde{V}'\}$$

where  $\tilde{V}' \subseteq \tilde{V}$ , using induction on the finite cardinality of  $\tilde{V}' \subseteq \tilde{V}$ .

If the cardinality of  $\tilde{V}'$  is 0, then  $\gamma(\tilde{\sqcap} \tilde{V}') = \sqcap \{\gamma(\tilde{v}) \mid \tilde{v} \in \tilde{V}'\}$  follows from condition 2. This proves the base case of the induction.

If the cardinality of  $\tilde{V}'$  is larger than 0, then  $\tilde{V}' = \tilde{V}'' \cup \{\tilde{v}''\}$  where  $\tilde{v}'' \notin \tilde{V}''$ ; which ensures that the cardinality of  $\tilde{V}''$  is strictly less than that of  $\tilde{V}'$ . Note that by condition 1,  $\gamma(\tilde{v} \tilde{\sqcap} \tilde{v}') = \gamma(\tilde{v}) \sqcap \gamma(\tilde{v}')$  also when  $\tilde{v} \tilde{\sqsubseteq} \tilde{v}' \vee \tilde{v}' \tilde{\sqsubseteq} \tilde{v}$ . Hence, by assuming that  $\gamma(\tilde{\sqcap} \tilde{V}'') = \sqcap \{\gamma(\tilde{v}) \mid \tilde{v} \in \tilde{V}''\}$  (this is the induction assumption),

$$\begin{aligned} \gamma(\tilde{\sqcap} \tilde{V}') &\stackrel{\text{calc.}}{=} \gamma((\tilde{\sqcap} \tilde{V}'') \tilde{\sqcap} \tilde{v}'') \\ &\stackrel{\text{cond. 1 and 3}}{=} \gamma(\tilde{\sqcap} \tilde{V}'') \sqcap \gamma(\tilde{v}'') \\ &\stackrel{\text{ind. ass.}}{=} (\sqcap \{\gamma(\tilde{v}) \mid \tilde{v} \in \tilde{V}''\}) \sqcap \gamma(\tilde{v}'') \\ &\stackrel{\text{calc.}}{=} \sqcap (\{\gamma(\tilde{v}) \mid \tilde{v} \in \tilde{V}''\} \cup \{\gamma(\tilde{v}'')\}) \\ &\stackrel{\text{calc.}}{=} \sqcap \{\gamma(\tilde{v}) \mid \tilde{v} \in \tilde{V}'\} \end{aligned}$$

which proves the lemma.  $\blacksquare$

### 3.2 Constructing Complete Lattices

There are several different ways to construct complete lattices. Any given set can be *lifted* into a complete lattice (Theorem 3.5).

**Theorem 3.5 (Complete lattice – Lifting):**

If  $S$  is a set, then  $\langle \mathcal{P}(S), \subseteq, \cup, \cap, \emptyset, S \rangle$  is a complete lattice.  $\square$

PROOF. Assume that  $S$  is a set and let  $S^{\mathcal{P}} \subseteq \mathcal{P}(S)$ . It is then trivially the case that  $\bigsqcup S^{\mathcal{P}} = \cup S^{\mathcal{P}}$ ,  $\bigsqcap S^{\mathcal{P}} = \cap S^{\mathcal{P}}$ ,  $\perp = \emptyset$  and  $\top = S$  if  $\sqsubseteq = \subseteq$  (note that  $\sqsubseteq$  is reflexive, transitive and anti-symmetric by definition).  $\blacksquare$

The *Cartesian product* of two complete lattices is a complete lattice (Theorem 3.6).

**Theorem 3.6 (Complete lattice – Cartesian product):**

If  $\langle V_1, \sqsubseteq_1, \bigsqcup_1, \bigsqcap_1, \perp_1, \top_1 \rangle$  and  $\langle V_2, \sqsubseteq_2, \bigsqcup_2, \bigsqcap_2, \perp_2, \top_2 \rangle$  are complete lattices, then so is  $\langle V, \sqsubseteq, \bigsqcup, \bigsqcap, \perp, \top \rangle$  where (let  $V' \subseteq V$ ):

$$\begin{aligned} V &= V_1 \times V_2 = \{(v_1, v_2) \mid v_1 \in V_1 \wedge v_2 \in V_2\} \\ (v_1, v_2) \sqsubseteq (v'_1, v'_2) &\iff v_1 \sqsubseteq_1 v'_1 \wedge v_2 \sqsubseteq_2 v'_2 \text{ where } v_1, v'_1 \in V_1 \text{ and } v_2, v'_2 \in V_2 \\ \bigsqcup V' &= (\bigsqcup_1 \{v_1 \in V_1 \mid \exists v_2 \in V_2 : (v_1, v_2) \in V'\}, \\ &\quad \bigsqcup_2 \{v_2 \in V_2 \mid \exists v_1 \in V_1 : (v_1, v_2) \in V'\}) \\ \bigsqcap V' &= (\bigsqcap_1 \{v_1 \in V_1 \mid \exists v_2 \in V_2 : (v_1, v_2) \in V'\}, \\ &\quad \bigsqcap_2 \{v_2 \in V_2 \mid \exists v_1 \in V_1 : (v_1, v_2) \in V'\}) \\ \perp &= (\perp_1, \perp_2) \\ \top &= (\top_1, \top_2) \end{aligned} \quad \square$$

PROOF. Assume that  $\langle V_1, \sqsubseteq_1, \bigsqcup_1, \bigsqcap_1, \perp_1, \top_1 \rangle$  and  $\langle V_2, \sqsubseteq_2, \bigsqcup_2, \bigsqcap_2, \perp_2, \top_2 \rangle$  are complete lattices and let  $V = \{(v_1, v_2) \mid v_1 \in V_1 \wedge v_2 \in V_2\}$  and  $(v_1, v_2) \sqsubseteq (v'_1, v'_2) \iff v_1 \sqsubseteq_1 v'_1 \wedge v_2 \sqsubseteq_2 v'_2$  where  $v_1, v'_1 \in V_1$  and  $v_2, v'_2 \in V_2$ . (Note that it is straightforward to verify that  $(V, \sqsubseteq)$  is a partially ordered set since  $\sqsubseteq_1$  and  $\sqsubseteq_2$  are partial orders.) Also assume that  $V' \subseteq V$ .

Since  $\bigsqcup_1 \{v_1 \in V_1 \mid \exists v_2 \in V_2 : (v_1, v_2) \in V'\} \sqsubseteq_1 v_1''$  for all upper bounds,  $v_1''$ , of  $\{v_1 \in V_1 \mid \exists v_2 \in V_2 : (v_1, v_2) \in V'\}$  and  $\bigsqcup_2 \{v_2 \in V_2 \mid \exists v_1 \in V_1 : (v_1, v_2) \in V'\} \sqsubseteq_2 v_2''$  for all upper bounds,  $v_2''$ , of  $\{v_2 \in V_2 \mid \exists v_1 \in V_1 : (v_1, v_2) \in V'\}$ , it is easy to see that  $\bigsqcup V' = (\bigsqcup_1 \{v_1 \in V_1 \mid \exists v_2 \in V_2 : (v_1, v_2) \in V'\}, \bigsqcup_2 \{v_2 \in V_2 \mid \exists v_1 \in V_1 : (v_1, v_2) \in V'\}) \sqsubseteq (v_1'', v_2'')$  (c.f., the definition of  $\sqsubseteq$  above).  $\bigsqcap V'$  is shown in a similar manner.

Since  $\perp_1 = \bigsqcup_1 \emptyset$  and  $\perp_2 = \bigsqcup_2 \emptyset$ , it is easy to see that  $\perp = (\bigsqcup_1 \emptyset, \bigsqcup_2 \emptyset) = (\perp_1, \perp_2)$ .  $\top$  is shown in a similar manner.  $\blacksquare$

A space of total functions where the domain of the functions is a set and the range is a complete lattice is itself a complete lattice (Theorem 3.7).

**Theorem 3.7 (Complete lattice – Total function space):**

If  $S$  is a set and  $\langle V_1, \sqsubseteq_1, \sqcup_1, \sqcap_1, \perp_1, \top_1 \rangle$  is a complete lattice, then  $\langle V, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$  where (let  $V' \subseteq V$ )

$$\begin{aligned} V &= S \rightarrow V_1 = \{f : S \rightarrow V_1 \mid f \text{ is a total function}\} \\ f \sqsubseteq f' &\iff \forall s \in S : f(s) \sqsubseteq_1 f'(s) \text{ where } f, f' \in V \\ \sqcup V' &= \lambda s \in S. \sqcup_1 \{f(s) \mid f \in V'\}, \\ \sqcap V' &= \lambda s \in S. \sqcap_1 \{f(s) \mid f \in V'\}, \\ \perp &= \lambda s \in S. \perp_1 \\ \top &= \lambda s \in S. \top_1 \end{aligned}$$

is also a complete lattice. □

PROOF. Assume that  $S$  is a set and  $\langle V_1, \sqsubseteq_1, \sqcup_1, \sqcap_1, \perp_1, \top_1 \rangle$  is a complete lattice,  $V = S \rightarrow V_1 = \{f : S \rightarrow V_1 \mid f \text{ is a total function}\}$  and  $f \sqsubseteq f' \iff \forall s \in S : f(s) \sqsubseteq_1 f'(s)$  where  $f, f' \in V$ . (Note that it is straightforward to verify that  $(V, \sqsubseteq)$  is a partially ordered set.) Also assume that  $V' \subseteq V$ . Note that the totality of  $f \in V$  will be implicitly used.

It is easy to see that  $\forall s \in S : \forall f' \in V' : f'(s) \sqsubseteq_1 \sqcup_1 \{f(s) \mid f \in V'\}$  and that  $\forall s \in S : \sqcup_1 \{f(s) \mid f \in V'\} \sqsubseteq_1 f''(s)$  for any  $f'' \in V$  such that  $\forall s \in S : \forall f' \in V' : f'(s) \sqsubseteq_1 f''(s)$  since  $\langle V_1, \sqsubseteq_1, \sqcup_1, \sqcap_1, \perp_1, \top_1 \rangle$  is a complete lattice. But, then it must be that  $\sqcup V' = \lambda s \in S. \sqcup_1 \{f(s) \mid f \in V'\}$  (c.f., the definition of  $\sqsubseteq$  above).  $\sqcap V'$  is shown in a similar manner.

Since  $\perp_1 = \sqcup_1 \emptyset$ , it is easy to see that  $\perp = \lambda s \in S. \sqcup_1 \emptyset = \lambda s \in S. \perp_1$ .  $\top$  is shown in a similar manner. ■

A space of monotone functions where both the domain and the range of the functions are complete lattices is itself a complete lattice (Theorem 3.8).

**Theorem 3.8 (Complete lattice – Monotone function space):**

If  $\langle V_1, \sqsubseteq_1, \sqcup_1, \sqcap_1, \perp_1, \top_1 \rangle$  and  $\langle V_2, \sqsubseteq_2, \sqcup_2, \sqcap_2, \perp_2, \top_2 \rangle$  are complete lattices,

then so is  $\langle V, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$  where (let  $V' \subseteq V$ ):

$$\begin{aligned}
V &= V_1 \rightarrow V_2 = \{f : V_1 \rightarrow V_2 \mid f \text{ is a monotone function}\} \\
f \sqsubseteq f' &\iff \forall v_1 \in V_1 : f(v_1) \sqsubseteq_2 f'(v_1) \text{ where } f, f' \in V \\
\sqcup V' &= \lambda v_1 \in V_1. \sqcup_2 \{f(v_1) \mid f \in V'\}, \\
\sqcap V' &= \lambda v_1 \in V_1. \sqcap_2 \{f(v_1) \mid f \in V'\}, \\
\perp &= \lambda v_1 \in V_1. \perp_2 \\
\top &= \lambda v_1 \in V_1. \top_2
\end{aligned}$$

□

PROOF. Similar to the proof of Theorem 3.7 with the addition that the monotonicity of  $f \in V$  gives that  $\forall v_1, v'_1 \in V_1 : v_1 \sqsubseteq_1 v'_1 \Rightarrow f(v_1) \sqsubseteq_2 f(v'_1)$  (c.f., Definition 3.1). ■

### 3.3 Galois Connections & Galois Insertions

The concrete semantics of a programming language can be abstracted in many different ways. The choice of abstraction is done by defining an *abstract domain*. A domain is, in general, a complete lattice, and an abstract domain is essentially the set of all possible abstract states that fit the definition of the domain. It is often shown that the abstract domain is a safe over-approximation of the *concrete domain* by deriving a *Galois connection* between the two domains [62]. A Galois connection between two domains (i.e., complete lattices),  $V$  and  $D$ , is described by an *abstraction function*,  $\alpha$ , and a *concretization function*,  $\gamma$ , which must fulfill the criterion in Definition 3.9.

**Definition 3.9 (Galois connection):**

$\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection iff  $\alpha$  and  $\gamma$  are monotone functions that fulfill

$$\begin{cases} \alpha \circ \gamma \sqsubseteq_D \lambda d. d \\ \gamma \circ \alpha \sqsupseteq_V \lambda v. v \end{cases}$$

for all  $v \in V$  and  $d \in D$ , where  $V$  is the concrete domain and  $D$  is the abstract domain. □

An often useful special case of a Galois connection is called a *Galois insertion*; c.f., Definition 3.10.

**Definition 3.10 (Galois insertion):**

$\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois insertion iff  $\alpha$  and  $\gamma$  are monotone functions that fulfill

$$\begin{cases} \alpha \circ \gamma = \lambda d.d \\ \gamma \circ \alpha \sqsupseteq_V \lambda v.v \end{cases}$$

for all  $v \in V$  and  $d \in D$ , where  $V$  is the concrete domain and  $D$  is the abstract domain.  $\square$

A function in the concrete domain,  $f : V \rightarrow V$ , can be safely approximated by a function in the abstract domain,  $\tilde{f} : D \rightarrow D$ , iff  $\forall d \in D : f(\gamma(d)) \sqsubseteq \gamma(\tilde{f}(d))$ . The best approximation is achieved by inducing  $f$  along  $\alpha$  [62]; c.f., Definition 3.11.

**Definition 3.11 (Induced function):**

Assuming that  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection, the best approximation,  $\tilde{f}$ , of  $f : V \rightarrow V$  in  $D \rightarrow D$  is given by:

$$\tilde{f} = \alpha \circ f \circ \gamma \quad \square$$

Sometimes, it is more convenient to work with adjunctions (c.f., Definition 3.12) instead of Galois connections.

**Definition 3.12 (Adjunction):**

$\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is said to be an adjunction between the complete lattices  $V = \langle V, \sqsubseteq_V, \sqcup_V, \sqcap_V, \perp_V, \top_V \rangle$  and  $D = \langle D, \sqsubseteq_D, \sqcup_D, \sqcap_D, \perp_D, \top_D \rangle$  iff  $\alpha$  and  $\gamma$  are total functions that satisfy

$$\alpha(v) \sqsubseteq_D d \iff v \sqsubseteq_V \gamma(d)$$

for all  $v \in V$  and  $d \in D$ .  $\square$

In fact, adjunctions are Galois connections (Theorem 3.13).

**Theorem 3.13 (Adjunctions and Galois connections):**

$\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is an adjunction iff it is a Galois connection.  $\square$

PROOF (c.f., [62]). First assume that  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is an adjunction. It will be proven that it also is a Galois connection by showing that  $\gamma \circ \alpha \sqsupseteq_V \lambda v.v$  and  $\alpha \circ \gamma \sqsubseteq_D \lambda d.d$ . For any  $v \in V$ , trivially  $\alpha(v) \sqsubseteq_D \alpha(v)$ . Using that  $\alpha(v) \sqsubseteq_D d \Rightarrow v \sqsubseteq_V \gamma(d)$ , it can be established that  $v \sqsubseteq_V \gamma(\alpha(v))$ . Similarly, for any  $d \in D$ , trivially  $\gamma(d) \sqsubseteq_V \gamma(d)$ . Using that  $v \sqsubseteq_V \gamma(d) \Rightarrow \alpha(v) \sqsubseteq_D d$ , it can

be established that  $\alpha(\gamma(d)) \sqsubseteq_D d$ . Thus,  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection.

Next assume that  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection. It will be proven that it also is an adjunction by showing that  $\alpha(v) \sqsubseteq_D d \Rightarrow v \sqsubseteq_V \gamma(d)$  and  $v \sqsubseteq_V \gamma(d) \Rightarrow \alpha(v) \sqsubseteq_D d$ . So, first assume that  $\alpha(v) \sqsubseteq_D d$ . Then, since  $\gamma$  is monotone,  $\gamma(\alpha(v)) \sqsubseteq_V \gamma(d)$ . Using that  $\gamma \circ \alpha \sqsupseteq_V \lambda v.v$ , it can be established that  $v \sqsubseteq_V \gamma(\alpha(v)) \sqsubseteq_V \gamma(d)$  as required. For the second part of the proof, assume that  $v \sqsubseteq_V \gamma(d)$ . Then, since  $\alpha$  is monotone,  $\alpha(v) \sqsubseteq_D \alpha(\gamma(d))$ . Using that  $\alpha \circ \gamma \sqsubseteq_D \lambda d.d$ , it can be established that  $\alpha(v) \sqsubseteq_D \alpha(\gamma(d)) \sqsubseteq_D d$  as required. ■

The abstraction and concretization functions are strictly related as described by Lemma 3.14.

**Lemma 3.14 (Relation between  $\alpha$  and  $\gamma$ ):**

If  $V = \langle V, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$  and  $\tilde{V} = \langle \tilde{V}, \tilde{\sqsubseteq}, \tilde{\sqcup}, \tilde{\sqcap}, \tilde{\perp}, \tilde{\top} \rangle$  are complete lattices, and  $\langle \alpha : V \rightarrow \tilde{V}, \gamma : \tilde{V} \rightarrow V \rangle$  is a Galois connection between these lattices, then ( $v \in V$  and  $\tilde{v} \in \tilde{V}$ ):

1.  $\alpha$  uniquely determines  $\gamma$  by  $\gamma(\tilde{v}) = \sqcup \{v \mid \alpha(v) \tilde{\sqsubseteq} \tilde{v}\}$  and  $\gamma$  uniquely determines  $\alpha$  by  $\alpha(v) = \tilde{\sqcap} \{\tilde{v} \mid v \sqsubseteq \gamma(\tilde{v})\}$ .
2.  $\alpha$  is completely additive and  $\gamma$  is completely multiplicative.

In particular,  $\alpha(\perp) = \tilde{\perp}$  and  $\gamma(\tilde{\top}) = \top$ . □

PROOF (c.f., [62]). Assume that  $V = \langle V, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$  and  $\tilde{V} = \langle \tilde{V}, \tilde{\sqsubseteq}, \tilde{\sqcup}, \tilde{\sqcap}, \tilde{\perp}, \tilde{\top} \rangle$  are complete lattices,  $\langle \alpha : V \rightarrow \tilde{V}, \gamma : \tilde{V} \rightarrow V \rangle$  is a Galois connection between these lattices,  $v \in V$  and  $\tilde{v} \in \tilde{V}$ .

To show 1, it will first be shown that  $\gamma$  is determined by  $\alpha$ . Since  $\langle \alpha : V \rightarrow \tilde{V}, \gamma : \tilde{V} \rightarrow V \rangle$  is an adjunction (Theorem 3.13), it must be that  $\gamma(\tilde{v}) = \sqcup \{v \mid v \sqsubseteq \gamma(\tilde{v})\} = \sqcup \{v \mid \alpha(v) \sqsubseteq \tilde{v}\}$ . Assume that both  $\langle \alpha, \gamma_1 \rangle$  and  $\langle \alpha, \gamma_2 \rangle$  are Galois connections, then  $\gamma_1(\tilde{v}) = \sqcup \{v \mid v \sqsubseteq \gamma_1(\tilde{v})\} = \sqcup \{v \mid \alpha(v) \sqsubseteq \tilde{v}\} = \sqcup \{v \mid v \sqsubseteq \gamma_2(\tilde{v})\} = \gamma_2(\tilde{v})$ , and thus,  $\gamma_1 = \gamma_2$ . This shows that  $\alpha$  uniquely determines  $\gamma$ . Similarly, it must be that  $\alpha(v) = \tilde{\sqcap} \{\tilde{v} \mid \alpha(v) \tilde{\sqsubseteq} \tilde{v}\} = \tilde{\sqcap} \{\tilde{v} \mid v \sqsubseteq \gamma(\tilde{v})\}$ . This shows that  $\gamma$  uniquely determines  $\alpha$ .

To show 2, consider  $V' \subseteq V$ , then

$$\begin{aligned} \alpha(\sqcup V') \tilde{\sqsubseteq} \tilde{v} &\stackrel{\text{Th. 3.13}}{\iff} \sqcup V' \sqsubseteq \gamma(\tilde{v}) \\ &\stackrel{\text{calc.}}{\iff} \forall v \in V' : v \sqsubseteq \gamma(\tilde{v}) \\ &\stackrel{\text{Th. 3.13}}{\iff} \forall v \in V' : \alpha(v) \sqsubseteq \tilde{v} \\ &\stackrel{\text{calc.}}{\iff} \tilde{\sqcap} \{\alpha(v) \mid v \in V'\} \tilde{\sqsubseteq} \tilde{v} \end{aligned}$$



and it follows that  $\alpha(\bigsqcup V') = \bigsqcup\{\alpha(v) \mid v \in V'\}$ .

The proof that  $\gamma(\bigsqcap \tilde{V}') = \bigsqcap\{\gamma(\tilde{v}) \mid \tilde{v} \in \tilde{V}'\}$  is analogous. ■

Thus, by Lemma 3.15, it suffices to specify either a completely additive abstraction function or a completely multiplicative concretization function in order to obtain a Galois connection.

**Lemma 3.15 (Galois connection – Existence):**

If  $V = \langle V, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$  and  $\tilde{V} = \langle \tilde{V}, \tilde{\sqsubseteq}, \tilde{\sqcup}, \tilde{\sqcap}, \tilde{\perp}, \tilde{\top} \rangle$  are complete lattices, and

1.  $\alpha: V \rightarrow \tilde{V}$  is completely additive, then there exists a  $\gamma: \tilde{V} \rightarrow V$  such that  $\langle \alpha, \gamma \rangle$  is a Galois connection.
2.  $\gamma: \tilde{V} \rightarrow V$  is completely multiplicative, then there exists an  $\alpha: V \rightarrow \tilde{V}$  such that  $\langle \alpha, \gamma \rangle$  is a Galois connection. □

PROOF (c.f., [62]). Assume that  $V = \langle V, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$  and  $\tilde{V} = \langle \tilde{V}, \tilde{\sqsubseteq}, \tilde{\sqcup}, \tilde{\sqcap}, \tilde{\perp}, \tilde{\top} \rangle$  are complete lattices,  $v \in V$  and  $\tilde{v} \in \tilde{V}$ .

To show 1, assume that  $\alpha$  is completely additive and define  $\gamma$  by:

$$\gamma(\tilde{v}) = \sqcup\{v' \mid \alpha(v') \tilde{\sqsubseteq} \tilde{v}\}$$

Then it must be that  $\alpha(v) \tilde{\sqsubseteq} \tilde{v} \Rightarrow v \in \{v' \mid \alpha(v') \tilde{\sqsubseteq} \tilde{v}\} \Rightarrow v \sqsubseteq \gamma(\tilde{v})$ , where the last implication follows from the definition of  $\gamma$ . For the other direction, first observe that  $v \sqsubseteq \gamma(\tilde{v}) \Rightarrow \alpha(v) \tilde{\sqsubseteq} \alpha(\gamma(\tilde{v}))$  since  $\alpha$  is completely additive and thus monotone. Then,

$$\begin{aligned} \alpha(\gamma(\tilde{v})) &= \alpha(\sqcup\{v' \mid \alpha(v') \tilde{\sqsubseteq} \tilde{v}\}) \\ &= \bigsqcup\{\alpha(v') \mid \alpha(v') \tilde{\sqsubseteq} \tilde{v}\} \\ &\tilde{\sqsubseteq} \tilde{v} \end{aligned}$$

and so  $v \sqsubseteq \gamma(\tilde{v}) \Rightarrow \alpha(v) \tilde{\sqsubseteq} \tilde{v}$ . Thus,  $\langle \alpha, \gamma \rangle$  is a Galois connection (Theorem 3.13).

The proof of 2 is similar. ■

### 3.4 Constructing Galois Connections

A Galois connection can be constructed in several ways. The following theorems (except Theorem 3.21) specify some of them.

The Cartesian product can be used to combine two existing Galois connections (Theorem 3.16).

**Theorem 3.16 (Galois connection – Independent attribute method):**

If  $\langle \alpha_1 : V_1 \rightarrow D_1, \gamma_1 : D_1 \rightarrow V_1 \rangle$  and  $\langle \alpha_2 : V_2 \rightarrow D_2, \gamma_2 : D_2 \rightarrow V_2 \rangle$  are Galois connections, then so is  $\langle \alpha : (V_1 \times V_2) \rightarrow (D_1 \times D_2), \gamma : (D_1 \times D_2) \rightarrow (V_1 \times V_2) \rangle$ , where

$$\begin{cases} \alpha((v_1, v_2)) = (\alpha_1(v_1), \alpha_2(v_2)) \\ \gamma((d_1, d_2)) = (\gamma_1(d_1), \gamma_2(d_2)) \end{cases}$$

and  $(v_1, v_2) \in V_1 \times V_2$  and  $(d_1, d_2) \in D_1 \times D_2$ .  $\square$

PROOF (c.f., [62]). Assume that  $\langle \alpha_1 : V_1 \rightarrow D_1, \gamma_1 : D_1 \rightarrow V_1 \rangle$  and  $\langle \alpha_2 : V_2 \rightarrow D_2, \gamma_2 : D_2 \rightarrow V_2 \rangle$  are Galois connections,  $(v_1, v_2) \in V_1 \times V_2$  and  $(d_1, d_2) \in D_1 \times D_2$ . Note that  $V_1 \times V_2$  and  $D_1 \times D_2$  are complete lattices (Theorem 3.6).

First calculate the following.

$$\begin{aligned} \alpha((v_1, v_2)) \sqsubseteq_D (d_1, d_2) &\stackrel{\text{Def. } \alpha}{\iff} (\alpha_1(v_1), \alpha_2(v_2)) \sqsubseteq_D (d_1, d_2) \\ &\stackrel{\text{calc.}}{\iff} \alpha_1(v_1) \sqsubseteq_{D_1} d_1 \wedge \alpha_2(v_2) \sqsubseteq_{D_2} d_2 \\ &\stackrel{\text{Th. 3.13}}{\iff} v_1 \sqsubseteq_{V_1} \gamma_1(d_1) \wedge v_2 \sqsubseteq_{V_2} \gamma_2(d_2) \\ &\stackrel{\text{calc.}}{\iff} (v_1, v_2) \sqsubseteq_V (\gamma_1(d_1), \gamma_2(d_2)) \\ &\stackrel{\text{Def. } \gamma}{\iff} (v_1, v_2) \sqsubseteq_V \gamma((d_1, d_2)) \end{aligned}$$

Then, using Theorem 3.13, the result follows.  $\blacksquare$

The Cartesian product can also be used on lifted sets (Theorem 3.17).

**Theorem 3.17 (Galois connection – Lifted independent attribute method):**

If  $\langle \alpha_1 : \mathcal{P}(V_1) \rightarrow D_1, \gamma_1 : D_1 \rightarrow \mathcal{P}(V_1) \rangle$  and  $\langle \alpha_2 : \mathcal{P}(V_2) \rightarrow D_2, \gamma_2 : D_2 \rightarrow \mathcal{P}(V_2) \rangle$  are Galois connections, then so is  $\langle \alpha : \mathcal{P}(V_1 \times V_2) \rightarrow (D_1 \times D_2), \gamma : (D_1 \times D_2) \rightarrow \mathcal{P}(V_1 \times V_2) \rangle$ , where

$$\begin{cases} \alpha(V) = (\alpha_1(\{v_1 \in V_1 \mid \exists v_2 \in V_2 : (v_1, v_2) \in V\}), \\ \quad \alpha_2(\{v_2 \in V_2 \mid \exists v_1 \in V_1 : (v_1, v_2) \in V\})) \\ \gamma((d_1, d_2)) = \gamma_1(d_1) \times \gamma_2(d_2) \end{cases}$$

and  $V \subseteq V_1 \times V_2$  and  $(d_1, d_2) \in D_1 \times D_2$ .  $\square$

PROOF. Assume that  $\langle \alpha_1 : \mathcal{P}(V_1) \rightarrow D_1, \gamma_1 : D_1 \rightarrow \mathcal{P}(V_1) \rangle$  and  $\langle \alpha_2 : \mathcal{P}(V_2) \rightarrow D_2, \gamma_2 : D_2 \rightarrow \mathcal{P}(V_2) \rangle$  are Galois connections,  $V \subseteq V_1 \times V_2$  and  $(d_1, d_2) \in D_1 \times D_2$ . Note that  $\mathcal{P}(V_1 \times V_2)$  and  $D_1 \times D_2$  are complete lattices (Theorems 3.5 and 3.6).

First, calculate

$$\begin{array}{lcl}
 \alpha(V) \sqsubseteq (d_1, d_2) & \stackrel{\text{Def. } \alpha}{\iff} & (\alpha_1(V'_1), \alpha_2(V'_2)) \sqsubseteq (d_1, d_2) \\
 & \stackrel{\text{calc.}}{\iff} & \alpha_1(V'_1) \sqsubseteq_1 d_1 \wedge \alpha_2(V'_2) \sqsubseteq_2 d_2 \\
 & \stackrel{\text{Th. 3.13}}{\iff} & V'_1 \subseteq \gamma_1(d_1) \wedge V'_2 \subseteq \gamma_2(d_2) \\
 & \stackrel{\text{calc.}}{\iff} & V'_1 \times V'_2 \subseteq \gamma_1(d_1) \times \gamma_2(d_2) \\
 & \stackrel{\text{Def. } \gamma}{\iff} & V'_1 \times V'_2 \subseteq \gamma((d_1, d_2)) \\
 \stackrel{V \subseteq V'_1 \times V'_2}{\iff} & & V \subseteq \gamma((d_1, d_2))
 \end{array}$$

where  $V'_1 = \{v_1 \in V_1 \mid \exists v_2 \in V_2 : (v_1, v_2) \in V\}$  and  $V'_2 = \{v_2 \in V_2 \mid \exists v_1 \in V_1 : (v_1, v_2) \in V\}$ . Then, using Theorem 3.13, the result follows. ■

Both the concrete and abstract domains of an existing Galois connection can be lifted to derive a new Galois connection (Theorem 3.20). Note that Lemmas 3.18 and 3.19 give that the specified abstraction and concretization functions are monotone.

**Lemma 3.18 (Monotonicity of  $\alpha_{\mathcal{P}}$ ):**

The function  $\alpha_{\mathcal{P}} : \mathcal{P}(V) \rightarrow \mathcal{P}(D)$ , defined as

$$\alpha_{\mathcal{P}}(V') = \{\alpha(v) \mid v \in V'\}$$

where  $V' \subseteq V$ ,  $\alpha$  is monotone and  $\alpha : V \rightarrow D$ , is monotone. □

PROOF. This proof amounts to showing that  $\forall V', V'' \in \mathcal{P}(V) : (V' \subseteq V'' \Rightarrow \alpha_{\mathcal{P}}(V') \subseteq \alpha_{\mathcal{P}}(V''))$ .

Assume that  $V', V'' \in \mathcal{P}(V)$  and that  $V' \subseteq V''$ . Then, by definition:

$$\begin{array}{l}
 \alpha_{\mathcal{P}}(V'') \stackrel{\text{Def. } \alpha_{\mathcal{P}}}{=} \{\alpha(v) \mid v \in V''\} \\
 \stackrel{\text{calc.}}{=} \{\alpha(v) \mid v \in V' \cup (V'' \setminus V')\} \\
 \stackrel{\text{calc.}}{=} \{\alpha(v) \mid v \in V'\} \cup \{\alpha(v) \mid v \in V'' \setminus V'\} \\
 \stackrel{\text{calc.}}{\supseteq} \{\alpha(v) \mid v \in V'\} \\
 \stackrel{\text{Def. } \alpha_{\mathcal{P}}}{=} \alpha_{\mathcal{P}}(V')
 \end{array}$$

where the rewriting of  $\alpha(V'')$  and the set splitting are possible since  $V' \subseteq V''$  and  $\alpha$  is monotone.

Thus, it has been shown that  $\alpha_{\mathcal{P}}$  is monotone. ■

**Lemma 3.19 (Monotonicity of  $\gamma_{\mathcal{P}}$ ):**

The function  $\gamma_{\mathcal{P}} : \mathcal{P}(D) \rightarrow \mathcal{P}(V)$ , defined as

$$\gamma_{\mathcal{P}}(D') = \{v \in V \mid \alpha(v) \in D'\}$$

where  $D' \subseteq D$ ,  $\alpha$  is monotone and  $\gamma : D \rightarrow V$ , is monotone.  $\square$

PROOF. This proof amounts to showing that  $\forall D', D'' \in \mathcal{P}(D) : (D' \subseteq D'' \Rightarrow \gamma_{\mathcal{P}}(D') \subseteq \gamma_{\mathcal{P}}(D''))$ .

Assume that  $D', D'' \in \mathcal{P}(D)$  and that  $D' \subseteq D''$ . Then, by definition:

$$\begin{aligned} \gamma_{\mathcal{P}}(D'') &\stackrel{\text{Def. } \gamma_{\mathcal{P}}}{=} \{v \in V \mid \alpha(v) \in D''\} \\ &\stackrel{\text{calc.}}{=} \{v \in V \mid \alpha(v) \in D' \cup (D'' \setminus D')\} \\ &\stackrel{\text{calc.}}{=} \{v \in V \mid \alpha(v) \in D'\} \cup \{v \in V \mid \alpha(v) \in D'' \setminus D'\} \\ &\stackrel{\text{calc.}}{\supseteq} \{v \in V \mid \alpha(v) \in D'\} \\ &\stackrel{\text{Def. } \gamma_{\mathcal{P}}}{=} \gamma_{\mathcal{P}}(D') \end{aligned}$$

where the rewriting of  $D''$  and the set splitting are possible since  $D' \subseteq D''$  and  $\alpha$  is monotone.

Thus,  $\gamma_{\mathcal{P}}(D') \subseteq \gamma_{\mathcal{P}}(D'')$ , and hence it has been shown that  $\gamma_{\mathcal{P}}$  is monotone.  $\blacksquare$

**Theorem 3.20 (Galois connection – Double lifting):**

If  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection, then so is  $\langle \alpha_{\mathcal{P}} : \mathcal{P}(V) \rightarrow \mathcal{P}(D), \gamma_{\mathcal{P}} : \mathcal{P}(D) \rightarrow \mathcal{P}(V) \rangle$ , where

$$\begin{cases} \alpha_{\mathcal{P}}(V') = \{\alpha(v) \mid v \in V'\} \\ \gamma_{\mathcal{P}}(D') = \{v \in V \mid \alpha(v) \in D'\} \end{cases}$$

and  $V' \subseteq V$  and  $D' \subseteq D$ .  $\square$

PROOF. Assume that  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection. Note that  $\mathcal{P}(V)$  and  $\mathcal{P}(D)$  are complete lattices (Theorem 3.5).

Since  $\alpha_{\mathcal{P}}$  and  $\gamma_{\mathcal{P}}$  are monotone (Lemmas 3.18 and 3.19, respectively), this proof amounts to showing that (c.f., Definition 3.9)

1.  $\gamma_{\mathcal{P}}(\alpha_{\mathcal{P}}(V')) \supseteq V'$
2.  $\alpha_{\mathcal{P}}(\gamma_{\mathcal{P}}(D')) \subseteq D'$

where  $V' \subseteq V$  and  $D' \subseteq D$ . Note that both cases trivially hold if  $V' = \emptyset$  or  $D' = \emptyset$ , which corresponds to the bottom elements in the two lattices. Therefore, assume that  $V' \neq \emptyset$  and  $D' \neq \emptyset$ .

For case 1, assume that  $V' \subseteq V$ . Then, by definition:

$$\gamma_{\mathcal{P}}(\alpha_{\mathcal{P}}(V')) = \{v \in V \mid \alpha(v) \in \{\alpha(v') \mid v' \in V'\}\}$$

Assume that  $v'' \in V'$ , then it must be that  $\alpha(v'') \in \{\alpha(v') \mid v' \in V'\}$ . But, then  $v'' \in \gamma_{\mathcal{P}}(\alpha_{\mathcal{P}}(V'))$  and thus  $\gamma_{\mathcal{P}}(\alpha_{\mathcal{P}}(V')) \supseteq V'$ .

For case 2, assume that  $D' \subseteq D$ . Then, by definition:

$$\alpha_{\mathcal{P}}(\gamma_{\mathcal{P}}(D')) = \{\alpha(v) \mid v \in \{v' \in V \mid \alpha(v') \in D'\}\}$$

Assume that  $d \in \alpha_{\mathcal{P}}(\gamma_{\mathcal{P}}(D'))$ . Then it must be that  $\exists v \in \{v' \in V \mid \alpha(v') \in D'\} : d = \alpha(v)$ . Hence, for that  $v$ , it must be that  $\alpha(v) \in D'$ , and therefore,  $d \in D'$ . Thus,  $\alpha_{\mathcal{P}}(\gamma_{\mathcal{P}}(D')) \subseteq D'$ . ■

It might be tempting to use the definition of  $\alpha_{\mathcal{P}}$  and  $\gamma_{\mathcal{P}}$  as given in Theorem 3.21, but as the theorem shows, this does *not* result in a Galois connection.

**Theorem 3.21 (Not a Galois connection – Double lifting):**

If  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection, then  $\langle \alpha'_{\mathcal{P}} : \mathcal{P}(V) \rightarrow \mathcal{P}(D), \gamma'_{\mathcal{P}} : \mathcal{P}(D) \rightarrow \mathcal{P}(V) \rangle$  is not a Galois connection, where

$$\begin{cases} \alpha'_{\mathcal{P}}(V') = \{\alpha(v) \mid v \in V'\} \\ \gamma'_{\mathcal{P}}(D') = \{\gamma(d) \mid d \in D'\} \end{cases}$$

and  $V' \subseteq V$  and  $D' \subseteq D$ . □

PROOF. Assume that  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection. From the definition of  $\alpha'_{\mathcal{P}}$  and  $\gamma'_{\mathcal{P}}$ , it clearly follows that they are monotone since  $\alpha$  and  $\gamma$  are (c.f., Lemma 3.18).

By way of contradiction, assume that  $\langle \alpha'_{\mathcal{P}}, \gamma'_{\mathcal{P}} \rangle$  is a Galois connection. Then, by Definition 3.9,  $\gamma'_{\mathcal{P}}(\alpha'_{\mathcal{P}}(V')) \supseteq V'$ . A closer look at  $\gamma'_{\mathcal{P}}(\alpha'_{\mathcal{P}}(V'))$  reveals that:

$$\gamma'_{\mathcal{P}}(\alpha'_{\mathcal{P}}(V')) = \{\gamma(d) \mid d \in \{\alpha(v) \mid v \in V'\}\}$$

Assume that  $v' \in V'$ , then  $v' \in \gamma'_{\mathcal{P}}(\alpha'_{\mathcal{P}}(V'))$  since  $\gamma'_{\mathcal{P}}(\alpha'_{\mathcal{P}}(V')) \supseteq V'$ . This means that  $\exists d' \in \{\alpha(v) \mid v \in V'\} : d' = \alpha(v')$  and hence, for this  $d'$ ,  $\exists v'' \in \{\gamma(d) \mid d \in \{\alpha(v) \mid v \in V'\}\} : v' = v'' = \gamma(d') = \gamma(\alpha(v'))$ .

But, since  $\langle \alpha, \gamma \rangle$  is a Galois connection,  $\gamma(\alpha(v')) \sqsupseteq v'$ . This means that it could be the case that  $\gamma(\alpha(v')) \sqsupset v'$ , and thus  $v' \neq v''$ , which means that  $\gamma'_{\mathcal{P}}(\alpha'_{\mathcal{P}}(V')) \not\supseteq V'$  is possible. Thus,  $\langle \alpha'_{\mathcal{P}}, \gamma'_{\mathcal{P}} \rangle$  is not a Galois connection. ■

The domains of a Galois connection can be extended to spaces of (total or monotone) functions (Theorem 3.22).

**Theorem 3.22 (Galois connection – Function space):**

If  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection, then so is  $\langle \alpha' : (S \rightarrow V) \rightarrow (S \rightarrow D), \gamma' : (S \rightarrow D) \rightarrow (S \rightarrow V) \rangle$  for some set,  $S$ , where:

$$\begin{cases} \alpha'(f) = \alpha \circ f \\ \gamma'(g) = \gamma \circ g \end{cases} \quad \square$$

PROOF (c.f., [62]). Assume that  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection and that  $S$  is a set. Note that  $S \rightarrow V$  and  $S \rightarrow D$  are complete lattices (Theorems 3.7 and 3.8).

First note that  $\alpha'$  and  $\gamma'$  are monotone since  $\alpha$  and  $\gamma$  are. Furthermore, since  $\langle \alpha, \gamma \rangle$  is a Galois connection,

$$\gamma'(\alpha'(f)) = \gamma \circ \alpha \circ f \sqsupseteq f$$

and

$$\alpha'(\gamma'(g)) = \alpha \circ \gamma \circ g \sqsubseteq g$$

and, thus, the theorem holds.  $\blacksquare$

A lifted concrete domain of a Galois connection can be extended to a lifted space of (total or monotone) functions when also extending the abstract domain (Theorem 3.24). Note that Lemma 3.23 gives that the concretization function is monotone.

**Lemma 3.23 (Monotonicity of  $\gamma_s$ ):**

The function  $\gamma_s : (S \rightarrow D) \rightarrow \mathcal{P}(S \rightarrow V)$ , defined as

$$\gamma_s(d) = \begin{cases} S \rightarrow V & \text{if } d = \tilde{\top} \\ \emptyset & \text{if } d = \tilde{\perp} \\ \{\lambda s \in S.v \mid v \in \gamma(d s)\} & \text{otherwise} \end{cases}$$

for some set  $S$  and complete lattices  $V$  and  $D$ , is monotone, given that  $\gamma : D \rightarrow \mathcal{P}(V)$  is a monotone function and  $d \in S \rightarrow D$ .  $\square$

PROOF. This proof amounts to showing that  $\forall d', d'' \in S \rightarrow D : (d' \sqsubseteq d'' \Rightarrow \gamma_s(d') \subseteq \gamma_s(d''))$ , which is trivially the case if  $d' = \tilde{\perp}$  or  $d'' = \tilde{\top}$ .

Assume that  $\gamma: D \rightarrow \mathcal{P}(V)$  is a monotone function,  $d', d'' \in S \rightarrow D$  and that  $d' \sqsubseteq d'' \wedge d' \neq \perp \wedge d'' \neq \top$ . Then, by definition:

$$\begin{cases} \gamma_s(d') = \{\lambda s \in S.v \mid v \in \gamma(d' s)\} \\ \gamma_s(d'') = \{\lambda s \in S.v \mid v \in \gamma(d'' s)\} \end{cases}$$

Since  $\gamma$  is monotone, it must be that  $\forall s \in S: \gamma(d' s) \subseteq \gamma(d'' s)$ . This means that

$$\begin{aligned} \gamma_s(d'') &= \{\lambda s \in S.v \mid v \in \gamma(d' s) \cup (\gamma(d'' s) \setminus \gamma(d' s))\} \\ &\supseteq \{\lambda s \in S.v \mid v \in \gamma(d' s)\} \cup \{\lambda s \in S.v \mid v \in (\gamma(d'' s) \setminus \gamma(d' s))\} \\ &= \gamma_s(d') \cup \{\lambda s \in S.v \mid v \in (\gamma(d'' s) \setminus \gamma(d' s))\} \end{aligned}$$

and thus, trivially,  $\gamma_s(d') \subseteq \gamma_s(d'')$ . ■

**Theorem 3.24 (Galois connection – Lifted function space):**

If  $\langle \alpha: \mathcal{P}(V) \rightarrow D, \gamma: D \rightarrow \mathcal{P}(V) \rangle$  is a Galois connection, then so is  $\langle \alpha_s: \mathcal{P}(S \rightarrow V) \rightarrow (S \rightarrow D), \gamma_s: (S \rightarrow D) \rightarrow \mathcal{P}(S \rightarrow V) \rangle$ , for some set  $S$ , where

$$\begin{cases} \alpha_s(V') = \begin{cases} \top & \text{if } V' = S \rightarrow V \\ \perp & \text{if } V' = \emptyset \\ \lambda s \in S. \alpha(\{v' s \mid v' \in V'\}) & \text{otherwise} \end{cases} \\ \gamma_s(d) = \begin{cases} S \rightarrow V & \text{if } d = \top \\ \emptyset & \text{if } d = \perp \\ \{\lambda s \in S.v \mid v \in \gamma(d s)\} & \text{otherwise} \end{cases} \end{cases}$$

and  $V' \subseteq S \rightarrow V$  and  $d \in S \rightarrow D$ . □

PROOF. Assume that  $\langle \alpha: \mathcal{P}(V) \rightarrow D, \gamma: D \rightarrow \mathcal{P}(V) \rangle$  is a Galois connection,  $S$  is a set,  $V' \subseteq S \rightarrow V$  and  $d \in S \rightarrow D$ . Note that  $\mathcal{P}(S \rightarrow V)$  and  $S \rightarrow D$  are complete lattices (Theorems 3.5, 3.7 and 3.8).

First note that:

$$\begin{aligned} \gamma_s(\alpha_s(S \rightarrow V)) &= \gamma_s(\top) = S \rightarrow V \supseteq S \rightarrow V \\ \gamma_s(\alpha_s(\emptyset)) &= \gamma_s(\perp) = \emptyset \supseteq \emptyset \\ \alpha_s(\gamma_s(\top)) &= \alpha_s(S \rightarrow V) = \top \sqsubseteq \top \\ \alpha_s(\gamma_s(\perp)) &= \alpha_s(\emptyset) = \perp \sqsubseteq \perp \end{aligned}$$

Then note that  $\gamma_s$  is monotone (Lemma 3.23) and calculate the following.

$$\begin{aligned}
 \alpha_s(V') \sqsubseteq d &\stackrel{\text{Def. } \alpha_s}{\iff} \lambda s \in S. \alpha(\{v' s \mid v' \in V'\}) \sqsubseteq d \\
 &\stackrel{\gamma_s \text{ mon.}}{\iff} \gamma_s(\lambda s \in S. \alpha(\{v' s \mid v' \in V'\})) \subseteq \gamma_s(d) \\
 &\stackrel{\text{Def. } \gamma_s}{\iff} \{\lambda s \in S. v \mid v \in \gamma(\lambda s' \in S. \alpha(\{v' s' \mid v' \in V'\})) s\} \subseteq \gamma_s(d) \\
 &\stackrel{\text{calc.}}{\iff} \{\lambda s \in S. v \mid v \in \gamma(\alpha(\{v' s' \mid v' \in V'\}))\} \subseteq \gamma_s(d) \\
 &\stackrel{\lambda v. v \sqsubseteq \gamma \circ \alpha}{\iff} \{\lambda s \in S. v \mid v \in \{v' s \mid v' \in V'\} \subseteq \\
 &\quad \{\lambda s \in S. v \mid v \in \gamma(\alpha(\{v' s' \mid v' \in V'\}))\}\} \subseteq \gamma_s(d) \\
 &\stackrel{\text{calc.}}{\iff} \{\lambda s \in S. v \mid v \in \{v' s \mid v' \in V'\}\} \subseteq \gamma_s(d) \\
 &\stackrel{\text{calc.}}{\iff} \{\lambda s \in S. (v' s) \mid v' \in V'\} \subseteq \gamma_s(d) \\
 &\stackrel{\text{calc.}}{\iff} \{v' \mid v' \in V'\} \subseteq \{\lambda s \in S. (v' s) \mid v' \in V'\} \subseteq \gamma_s(d) \\
 &\stackrel{\text{calc.}}{\iff} \{v' \mid v' \in V'\} \subseteq \gamma_s(d) \\
 &\stackrel{\text{calc.}}{\iff} V' \subseteq \gamma_s(d)
 \end{aligned}$$

Then, using Theorem 3.13, the result follows. ■

The domains of a Galois connection can be indexed with the elements from some set (Theorem 3.25).

**Theorem 3.25 (Galois connection – Indexing):**

If  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection, then so is  $\langle \alpha' : (S \times V) \rightarrow (S \times D), \gamma' : (S \times D) \rightarrow (S \times V) \rangle$ , for some set  $S \ni s$  (with the partial order =), where

$$\begin{cases} \alpha'((s, v)) = (s, \alpha(v)) \\ \gamma'((s', d)) = (s', \gamma(d)) \end{cases}$$

and  $(s, v) \in S \times V$  and  $(s', d) \in S \times D$ . The top elements,  $\top'_V$  and  $\top'_D$ , correspond to the elements  $(s, v)$  and  $(s, d)$  for some  $s \in S$ , respectively, where  $\alpha(v) = \top_D$  and  $\gamma(d) = \top_V$ . The bottom elements are defined in a corresponding manner.

$\alpha'$  and  $\gamma'$  for  $\langle \alpha' : (V \times S) \rightarrow (D \times S), \gamma' : (D \times S) \rightarrow (V \times S) \rangle$  are defined similarly. □

PROOF. Assume that  $\langle \alpha : V \rightarrow D, \gamma : D \rightarrow V \rangle$  is a Galois connection,  $S$  is a set,  $(s, v) \in S \times V$  and  $(s', d) \in S \times D$ .



First note that:

$$\begin{aligned}
 \gamma'(\alpha'(\top'_V)) &= \gamma'(\tilde{\top}'_D) = \top'_V \sqsupseteq'_V \top'_V \\
 \gamma'(\alpha'(\perp'_V)) &= \gamma'(\tilde{\perp}'_D) = \perp'_V \sqsupseteq'_V \perp'_V \\
 \alpha'(\gamma'(\tilde{\top}'_D)) &= \alpha'(\top'_V) = \tilde{\top}'_D \sqsubseteq'_D \tilde{\top}'_D \\
 \alpha'(\gamma'(\tilde{\perp}'_D)) &= \alpha'(\perp'_V) = \tilde{\perp}'_D \sqsubseteq'_D \tilde{\perp}'_D
 \end{aligned}$$

Then, calculate the following.

$$\begin{aligned}
 \alpha'((s, v)) \sqsubseteq_{SD} (s', d) &\stackrel{\text{Def. } \alpha'}{\iff} (s, \alpha(v)) \sqsubseteq_{SD} (s', d) \\
 &\stackrel{\text{calc.}}{\iff} s = s' \wedge \alpha(v) \sqsubseteq_D d \\
 &\stackrel{\text{Th. 3.13}}{\iff} s = s' \wedge v \sqsubseteq_V \gamma(d) \\
 &\stackrel{\text{calc.}}{\iff} (s, v) \sqsubseteq_{SV} (s', \gamma(d)) \\
 &\stackrel{\text{Def. } \gamma'}{\iff} (s, v) \sqsubseteq_{SV} \gamma'((s', d))
 \end{aligned}$$

Now, using Theorem 3.13, the result follows.

The proof for  $\langle \alpha' : (V \times S) \rightarrow (D \times S), \gamma' : (D \times S) \rightarrow (V \times S) \rangle$  being a Galois connection is conducted analogously. ■

### 3.5 Constructing Galois Insertions

A Galois insertion  $\langle \alpha, \gamma \rangle$  between two domains,  $D$  and  $\tilde{D}$ , can be constructed by following steps 1-5 below [23].

1. A domain,  $D$ , with a partial order,  $\sqsubseteq$ , a least (bottom) element,  $\perp$ , a greatest (top) element,  $\top$ , a greatest lower bound,  $\sqcap$ , and a least upper bound,  $\sqcup$ , so that  $\langle D, \sqsubseteq, \sqcup, \sqcap, \perp, \top \rangle$  is a complete lattice must be given.
2. Define a domain  $\tilde{D}$  and a monotone concretization function  $\gamma : \tilde{D} \rightarrow D$ .
3. Define the partial order  $\tilde{\sqsubseteq}$  for  $\tilde{D}$ .
4. The greatest lower bound  $\tilde{\sqcap}$  and the least upper bound  $\tilde{\sqcup}$  must exist for all subsets of  $\tilde{D}$ . Then, by definition,  $\langle \tilde{D}, \tilde{\sqsubseteq}, \tilde{\sqcup}, \tilde{\sqcap}, \tilde{\perp}, \tilde{\top} \rangle$  is a complete lattice.
5. Define the abstraction function  $\alpha : D \rightarrow \tilde{D}$ , which must be monotone.

Assuming that the domains  $D$  and  $\tilde{D}$  and the monotone concretization function,  $\gamma$ , are defined, the partial ordering  $\tilde{\sqsubseteq}$  can easily be defined as given by Definition 3.26 [23].

**Definition 3.26 (Partial order):**

$\underline{\subseteq}$  is a partial order for the domain  $\tilde{D}$  iff  $\forall \tilde{d}_1, \tilde{d}_2 \in \tilde{D} : (\tilde{d}_1 \underline{\subseteq} \tilde{d}_2 \iff \gamma(\tilde{d}_1) \subseteq \gamma(\tilde{d}_2))$ .  $\square$

Based on this definition of the partial order, the greatest lower bound and least upper bound can be defined as given by Definitions 3.27 and 3.28, respectively [23].

**Definition 3.27 (Greatest lower bound):**

The element  $\tilde{d} \in \tilde{D}$  is a lower bound of  $\tilde{D}' \subseteq \tilde{D}$  iff  $\forall \tilde{d}' \in \tilde{D}' : \tilde{d} \underline{\subseteq} \tilde{d}'$ . The element  $\tilde{d} \in \tilde{D}$  is the greatest lower bound of  $\tilde{D}' \subseteq \tilde{D}$  ( $\tilde{d} = \tilde{\bigcap} \tilde{D}'$ ) iff  $\tilde{d}$  is a lower bound of  $\tilde{D}'$  and for all other lower bounds  $\tilde{d}'$  of  $\tilde{D}'$ ,  $\tilde{d}' \underline{\subseteq} \tilde{d}$ .  $\square$

**Definition 3.28 (Least upper bound):**

The element  $\tilde{d} \in \tilde{D}$  is an upper bound of  $\tilde{D}' \subseteq \tilde{D}$  iff  $\forall \tilde{d}' \in \tilde{D}' : \tilde{d}' \underline{\subseteq} \tilde{d}$ . The element  $\tilde{d} \in \tilde{D}$  is the least upper bound of  $\tilde{D}' \subseteq \tilde{D}$  ( $\tilde{d} = \tilde{\bigcup} \tilde{D}'$ ) iff  $\tilde{d}$  is an upper bound of  $\tilde{D}'$  and for all other upper bounds  $\tilde{d}'$  of  $\tilde{D}'$ ,  $\tilde{d} \underline{\subseteq} \tilde{d}'$ .  $\square$

The abstraction function  $\alpha$  can be defined based on the definition of the greatest lower bound operator as given by Definition 3.29 [23].

**Definition 3.29 (Abstraction function,  $\alpha$ ):**

Given two domains  $D$  and  $\tilde{D}$  and a monotone concretization function  $\gamma : \tilde{D} \rightarrow D$ , the abstraction function  $\alpha : D \rightarrow \tilde{D}$  is defined by:

$$\alpha(d) = \tilde{\bigcap} \{ \tilde{d} \mid d \subseteq \gamma(\tilde{d}) \}$$

where  $d \in D$  and  $\tilde{d} \in \tilde{D}$ .  $\square$

Alternatively, assuming that two domains and a monotone abstraction function have been defined, the concretization function  $\gamma$  can be defined based on the least upper bound operator as given by Definition 3.30 [23].

**Definition 3.30 (Alternative definition – Concretization function,  $\gamma$ ):**

Given two domains  $D$  and  $\tilde{D}$  and a monotone abstraction function  $\alpha : D \rightarrow \tilde{D}$ , the concretization function  $\gamma : \tilde{D} \rightarrow D$  is defined by:

$$\gamma(\tilde{d}) = \bigcup \{ d \mid \alpha(d) \underline{\subseteq} \tilde{d} \}$$

where  $d \in D$  and  $\tilde{d} \in \tilde{D}$ .  $\square$

### 3.6 The Interval Domain

One example of an abstract domain for values is the interval domain [19, 23, 62]. The definition of an interval is given in Definition 3.31.

**Definition 3.31 (Interval):**

An interval is defined as  $[n_1, n_2]$ , where  $n_1, n_2 \in \mathbf{Val} = \mathbb{Z} \cup \{-\infty, \infty\}$  are the lower and upper bounds of the interval, respectively, and  $n_1 \leq n_2$ . Formally, the set of all intervals is defined as  $\mathbf{Intv} = \{\perp_{int}, \top_{int}\} \cup \{[n_1, n_2] \mid n_1 \leq n_2 \wedge n_1, n_2 \in \mathbf{Val}\}$ , where  $\perp_{int}$  denotes an invalid interval and  $\top_{int}$  is greater than any other element of  $\mathbf{Intv}$ .  $\square$

A Galois insertion will now be created between  $\mathcal{P}(\mathbf{Val})$  and  $\mathbf{Intv}$ , using the steps of Section 3.5. The concretization function  $\gamma_{int} : \mathbf{Intv} \rightarrow \mathcal{P}(\mathbf{Val})$  is given by Definition 3.32.

**Definition 3.32 (concretization of intervals):**

$$\gamma_{int}(i) = \begin{cases} \mathbb{Z} \cup \{-\infty, \infty\} & \text{if } i = \top_{int} \\ \emptyset & \text{if } i = \perp_{int} \\ \{n \in \mathbf{Val} \mid n_1 \leq n \leq n_2\} & \text{otherwise (i.e., } i = [n_1, n_2]) \end{cases} \quad \square$$

The partial order relation for intervals,  $\sqsubseteq_{int}$ , is given by Definition 3.33 (using Definition 3.26).

**Definition 3.33 (Partial order for intervals):**

$$\begin{cases} i \sqsubseteq_{int} \top_{int} \\ \perp_{int} \sqsubseteq_{int} i \\ [n_1, n_2] \sqsubseteq_{int} [n'_1, n'_2] \iff n'_1 \leq n_1 \wedge n_2 \leq n'_2 \end{cases} \quad \square$$

The greatest lower bound operator for intervals  $\sqcap_{int}$  is defined as given by Definition 3.34 (using Definition 3.27).

**Definition 3.34 (Greatest lower bound for intervals):**

$$\begin{cases} i \sqcap_{int} \top_{int} = \top_{int} \sqcap_{int} i = i \\ i \sqcap_{int} \perp_{int} = \perp_{int} \sqcap_{int} i = \perp_{int} \\ [n_1, n_2] \sqcap_{int} [n'_1, n'_2] = \begin{cases} [\max(\{n_1, n'_1\}), \min(\{n_2, n'_2\})] & \text{if } \max(\{n_1, n'_1\}) \leq \min(\{n_2, n'_2\}) \\ \perp_{int} & \text{otherwise} \end{cases} \end{cases} \quad \square$$

The least upper bound operator for intervals  $\sqcup_{int}$  is defined as given by Definition 3.35 (using Definition 3.28).

**Definition 3.35 (Least upper bound for intervals):**

$$\begin{cases} i \sqcup_{int} \top_{int} = \top_{int} \sqcup_{int} i = \top_{int} \\ i \sqcup_{int} \perp_{int} = \perp_{int} \sqcup_{int} i = i \\ [n_1, n_2] \sqcup_{int} [n'_1, n'_2] = [\min(\{n_1, n'_1\}), \max(\{n_2, n'_2\})] \end{cases} \quad \square$$

The abstraction function  $\alpha_{int} : \mathcal{P}(\mathbf{Val}) \rightarrow \mathbf{Intv}$  is defined as given by Definition 3.36 (using Definition 3.29).

**Definition 3.36 (Abstraction to interval):**

$$\alpha_{int}(V) = \begin{cases} \top_{int} & \text{if } V = \mathbb{Z} \cup \{-\infty, \infty\} \\ \perp_{int} & \text{if } V = \emptyset \\ [\min(V), \max(V)] & \text{otherwise} \end{cases} \quad \square$$

To show that  $\langle \alpha_{int}, \gamma_{int} \rangle$  is a Galois insertion, it would suffice to show that  $\gamma_{int}$  is monotone, since the steps of Section 3.5 have been used. However, for clarity, the entire proof is given in the proof of Theorem 3.39. Note that Lemmas 3.37 and 3.38 give that  $\gamma_{int}$  and  $\alpha_{int}$ , respectively, are monotone.

**Lemma 3.37 (Monotonicity of  $\gamma_{int}$ ):**

The function  $\gamma_{int} : \mathbf{Intv} \rightarrow \mathcal{P}(\mathbf{Val})$  is monotone. □

PROOF. It should be shown that  $\forall i, i' \in \mathbf{Intv} : (i \sqsubseteq_{int} i' \Rightarrow \gamma_{int}(i) \subseteq \gamma_{int}(i'))$ . Note that the proof is trivial for the case that  $i = \perp_{int}$  or  $i' = \top_{int}$ .

Assume that  $i = [n_1, n_2] \in \mathbf{Intv}$  and  $i' = [n'_1, n'_2] \in \mathbf{Intv}$ , such that  $i \sqsubseteq_{int} i'$ . Further assume that  $n \in \gamma_{int}(i)$ . Then it must be the case that  $n_1 \leq n \leq n_2$  (Definition 3.32). Since  $i \sqsubseteq_{int} i'$ , it must be the case that  $n'_1 \leq n_1 \leq n \leq n_2 \leq n'_2$  (Definition 3.33). But, then it must be that  $n \in \gamma_{int}(i')$  (Definition 3.32), and thus,  $\gamma_{int}(i) \subseteq \gamma_{int}(i')$ . ■

**Lemma 3.38 (Monotonicity of  $\alpha_{int}$ ):**

The function  $\alpha_{int} : \mathcal{P}(\mathbf{Val}) \rightarrow \mathbf{Intv}$  is monotone. □

PROOF. It should be shown that  $\forall V, V' \in \mathcal{P}(\mathbf{Val}) : (V \subseteq V' \Rightarrow \alpha_{int}(V) \sqsubseteq_{int} \alpha_{int}(V'))$ . Note that the proof is trivial for the case that  $V = \emptyset$  or  $V' = \mathbb{Z} \cup \{-\infty, \infty\}$ .

Assume that  $V, V' \in \mathcal{P}(\mathbf{Val})$ , such that  $V \subseteq V'$ . Further assume that  $\alpha_{int}(V) = [n_1, n_2]$  and  $\alpha_{int}(V') = [n'_1, n'_2]$ . Since  $V \subseteq V'$ , it must be that  $\forall v \in V : \{v\} \subseteq V'$ , and hence,  $\{n_1, n_2\} \subseteq V'$ . But then, it must be that  $\min(V') = n'_1 \leq n_1 = \min(V)$  and  $\max(V) = n_2 \leq n'_2 = \max(V')$ , and thus,  $[n_1, n_2] \sqsubseteq_{int} [n'_1, n'_2]$  (Definition 3.33), which means that  $\alpha_{int}(V) \sqsubseteq_{int} \alpha_{int}(V')$ . ■

**Theorem 3.39 (Galois insertion – Intervals):**

$\langle \alpha_{int} : \mathcal{P}(\mathbf{Val}) \rightarrow \mathbf{Intv}, \gamma_{int} : \mathbf{Intv} \rightarrow \mathcal{P}(\mathbf{Val}) \rangle$  is a Galois insertion. □

PROOF. The proof amounts to showing that the constraints in Definition 3.10 are fulfilled by  $\langle \alpha_{int}, \gamma_{int} \rangle$ . Note that  $\mathcal{P}(\mathbf{Val})$  and  $\mathbf{Intv}$  are complete lattices [62].

According to Lemmas 3.37 and 3.38,  $\gamma_{int}$  and  $\alpha_{int}$  are monotone. To show that  $\alpha_{int}(\gamma_{int}(i)) = i$ , assume that  $i \in \mathbf{Intv}$ .

- If  $i = \top_{int}$ , then  $\gamma_{int}(i) = \mathbb{Z} \cup \{-\infty, \infty\}$ . Thus,  $\alpha_{int}(\gamma_{int}(i)) = \alpha_{int}(\mathbb{Z} \cup \{-\infty, \infty\}) = \top_{int} = i$ .
- If  $i = \perp_{int}$ , then  $\gamma_{int}(i) = \emptyset$ . Thus,  $\alpha_{int}(\gamma_{int}(i)) = \alpha_{int}(\emptyset) = \perp_{int} = i$ .
- Otherwise (i.e., if  $i = [n_1, n_2]$ ) then  $\gamma_{int}(i) = \{n \in \mathbf{Val} \mid n_1 \leq n \leq n_2\}$ . Thus,  $\alpha_{int}(\gamma_{int}(i)) = \alpha_{int}(\{n \in \mathbf{Val} \mid n_1 \leq n \leq n_2\}) = [n_1, n_2] = i$ .

To show that  $\gamma_{int}(\alpha_{int}(V)) \supseteq V$ , assume that  $V \in \mathcal{P}(\mathbf{Val})$ .

- If  $V = \mathbb{Z} \cup \{-\infty, \infty\}$ , then  $\alpha_{int}(V) = \top_{int}$ . Thus,  $\gamma_{int}(\alpha_{int}(V)) = \gamma_{int}(\top_{int}) = \mathbb{Z} \cup \{-\infty, \infty\} \supseteq \mathbb{Z} \cup \{-\infty, \infty\} = V$ .
- If  $V = \emptyset$ , then  $\alpha_{int}(V) = \perp_{int}$ . Thus,  $\gamma_{int}(\alpha_{int}(V)) = \gamma_{int}(\perp_{int}) = \emptyset \supseteq \emptyset = V$ .
- Otherwise,  $\alpha_{int}(V) = [\min(V), \max(V)]$ . Thus,  $\gamma_{int}(\alpha_{int}(V)) = \gamma_{int}([\min(V), \max(V)]) = \{n \in \mathbf{Val} \mid \min(V) \leq n \leq \max(V)\} \supseteq V$ . ■



## Chapter 4

# PPL: A Parallel Programming Language

In this chapter, PPL, a parallel programming language will be defined. The parallel entity of execution is referred to as a thread.

PPL provides both thread-private and globally shared memory, referred to as registers,  $r \in \mathbf{Reg}$ , and variables,  $x \in \mathbf{Var}$ , respectively, and arithmetical operations etc. within a thread can be performed using the values of the thread's registers. PPL also provides shared resources, referred to as locks,  $lck \in \mathbf{Lck}$ , that can be acquired in a mutually exclusive manner by the threads. The operations (statements) provided by the instruction set may have variable execution times. (C.f., multi-core CPUs, which have both local and global memory, a shared memory bus and atomic, i.e., mutually exclusive, operations.)

NOTE. *A summary of the notation and nomenclature used in this thesis can be found in Appendix A.*

The syntax of PPL, which is a set of operations using the discussed architectural features, is defined in Table 4.1.  $\Pi \in \mathbf{Prg}$  denotes a program, which simply is a set of threads, i.e.,  $\Pi = \mathbf{Thrd} \in \mathcal{P}(\mathbf{ThrdID} \times \mathbf{Stm}) = \mathbf{Prg}$ , where each thread,  $T \in \mathbf{Thrd}$ , is a pair of a unique identifier,  $d \in \mathbf{ThrdID}$ , and a statement,  $s \in \mathbf{Stm}$ . This makes every thread unique and distinguishable from other

$$\begin{aligned}
\Pi &::= \{T_1, \dots, T_m\} \\
T &::= (d, s) \\
s &::= [\text{halt}]^l \mid [\text{skip}]^l \mid [r := a]^l \mid [\text{if } b \text{ goto } l']^l \mid [\text{load } r \text{ from } x]^l \mid \\
&\quad [\text{store } r \text{ to } x]^l \mid [\text{lock } lck]^l \mid [\text{unlock } lck]^l \mid s_1 ; s_2 \\
a &::= n \mid r \mid a_1 + a_2 \mid a_1 - a_2 \mid a_1 * a_2 \mid a_1 / a_2 \\
b &::= \text{true} \mid \text{false} \mid !b \mid b_1 \ \&\& \ b_2 \mid a_1 == a_2 \mid a_1 <= a_2
\end{aligned}$$

Table 4.1: The Syntax of PPL.

threads, even if several threads consist of the same statement. To increase the readability of the semantics, it will be assumed that the axiom-statements (all statements except the sequentially composed statement,  $s_1 ; s_2$ ) of each thread are uniquely labeled with consecutive labels,  $l \in \mathbf{Lbl}$ , and stored in an array-like fashion in ascending order of their labels.  $a \in \mathbf{Aexp}$  and  $b \in \mathbf{Bexp}$  denote an arithmetic and a boolean expression, respectively, and  $n \in \mathbf{Val}$  is an integer value.

Locks can be acquired in a mutually exclusive manner using `lock` and released using `unlock`. Values can be transferred between variables and registers using `load` and `store`. Conditional branching is performed using `if`. A register is assigned a value using `:=`. A no-operation is performed using `skip`. And, `halt` stops the execution of the issuing thread. `halt` must be the last statement of each thread in the program, but it could also occur anywhere “within” a thread. The semantics of PPL is formally defined in Section 4.2.

## 4.1 States & Configurations

A number of sub-states will be used when expressing how a set of given statements affects the state of the entire system when the statements are executed in parallel; i.e., when expressing the semantics of PPL. For each thread,  $T$ , of a program, there is an instance of the following states.

$pc_T$  :  $\mathbf{Lbl}_T$  – a program counter that keeps track of which statement within the thread  $T$  that is active.



NOTE. The tuple  $\langle pc_{T_1}, \dots, pc_{T_m} \rangle$ , assuming that  $\mathbf{Thrd} = \{T_1, \dots, T_m\}$ , defines a unique program point.

$\mathbb{R}_T : \mathbf{Reg}_T \rightarrow \mathbf{Val}$  – a mapping from T’s registers to their values.

$t_T^a : \mathbf{Time}$  – an absolute point in discrete time when the previous statement in T was executed.

For the program as such, there is an instance of the following states.

$\mathbb{x} : \mathbf{Var} \rightarrow \mathbf{Thrd} \rightarrow \mathcal{P}(\mathbf{Val} \times \mathbf{Time})$  – a mapping from variables to a set of writes; i.e., a pair of a value and an absolute point in time.

$\mathbb{l} : \mathbf{Lck} \rightarrow (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time})$  – a mapping from locks to their values; i.e., a state ( $\mathbf{Lck}_{\text{stt}} = \{\text{unlocked}, \text{locked}\}$ ), a current owner ( $\mathbf{Thrd}_{\perp} = \mathbf{Thrd} \cup \{\perp_{\text{thrd}}\}$ ), an absolute point in time when the lock must be taken by the current owner, a previous owner, and an absolute point in time when the lock was last released. For the case that no thread owns the lock, the owner is  $\perp_{\text{thrd}}$ .

NOTE. The only information about locks that is needed in the concrete case is the current owner of each lock (c.f., Tables 4.2 and 4.3). The rest of the information is only necessary when expressing the abstract semantics (c.f., Chapter 5). However, the soundness of the abstract semantics is easier proven if this information is included in the concrete case as well.

The types of the states  $\mathbb{x}$  and  $\mathbb{l}$  might look a bit peculiar at first glance; the need for their definitions will become apparent when defining an abstract interpretation of the PPL semantics in Section 5.8.

The above listed states, together with the threads of the program, will be referred to as a program state or configuration,  $c \in \mathbf{Conf}$ .  $\mathbf{Conf}$  and  $c$  are defined as follows.

$$\begin{aligned} \mathbf{Conf} ::= & \mathcal{P}_{T \in \mathbf{Thrd}}(\{T\} \times \mathbf{Lbl}_T \times (\mathbf{Reg}_T \rightarrow \mathbf{Val}) \times \mathbf{Time}) \times \\ & (\mathbf{Var} \rightarrow \mathbf{Thrd} \rightarrow \mathcal{P}(\mathbf{Val} \times \mathbf{Time})) \times \\ & (\mathbf{Lck} \rightarrow (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time})) \end{aligned}$$

$$c ::= \langle [T, pc_T, r_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle$$

Since it is not possible to beforehand determine the number of threads specified by a program,  $\mathcal{P}_{T \in \mathbf{Thrd}}(\dots)$  is defined to expand to  $|\mathbf{Thrd}|$  instances (i.e., one instance for each thread,  $T$ , in a given program) of type  $\{T\} \times \mathbf{Lbl}_T \times (\mathbf{Reg}_T \rightarrow \mathbf{Val}) \times \mathbf{Time}$ . Likewise,  $[\dots]_{T \in \mathbf{Thrd}}$  is defined to expand in the corresponding manner. This way,  $c \in \mathbf{Conf}$  can be regarded as a tuple with a known size when the number of threads in a program is known.

Sub-components of a configuration will also be of interest when considering single threads (see Table 4.2). Therefore, the following “smaller” configurations,  $c_{in}^{ax} \in \mathbf{Conf}_{in}^{ax}$  and  $c_{out}^{ax} \in \mathbf{Conf}_{out}^{ax}$ , are defined for  $T \in \mathbf{Thrd}$ .

$$\begin{aligned} \mathbf{Conf}_{in}^{ax} = & \{T\} \times \mathbf{Lbl}_T \times (\mathbf{Reg}_T \rightarrow \mathbf{Val}) \times \\ & (\mathbf{Var} \rightarrow \mathbf{Thrd} \rightarrow \mathcal{P}(\mathbf{Val} \times \mathbf{Time})) \times \\ & (\mathbf{Lck} \rightarrow (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time})) \\ & \times \mathbf{Time} \end{aligned}$$

$$c_{in}^{ax} ::= \langle T, pc, r, \mathbb{x}, \mathbb{l}, t \rangle$$

$$\begin{aligned} \mathbf{Conf}_{out}^{ax} = & \mathbf{Lbl}_T \times (\mathbf{Reg}_T \rightarrow \mathbf{Val}) \times \\ & (\mathbf{Var} \rightarrow \mathbf{Thrd} \rightarrow \mathcal{P}(\mathbf{Val} \times \mathbf{Time})) \times \\ & (\mathbf{Lck} \rightarrow (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time})) \end{aligned}$$

$$c_{out}^{ax} ::= \langle pc, r, \mathbb{x}, \mathbb{l} \rangle$$

## 4.2 Semantics

The semantic rules for individual statements within a thread, the language axioms, are described by the relation  $\xrightarrow{ax} : \mathbf{Conf}_{in}^{ax} \times \mathbf{Conf}_{out}^{ax} \rightarrow \{\mathbf{true}, \mathbf{false}\}$ , which is formally defined in Table 4.2. The semantic rule for a set of threads (i.e., the program) is described by the relation  $\xrightarrow{prg} : \mathbf{Conf} \times \mathbf{Conf} \rightarrow \{\mathbf{true}, \mathbf{false}\}$ , which is defined based on  $\xrightarrow{ax}$  as given in Table 4.3. Note that the functions STM and STT, OWN, DL, POWN and REL are defined in Tables 4.4 and 4.5, respectively. Note that STM is a total function.

$\xrightarrow{ax}$  and  $\xrightarrow{prg}$  are relations, not functions, because one single input configuration can have several outputs; e.g., if two or more threads execute `lock lck`, where  $\text{STT}(\mathbb{l} \text{ lck}) = \text{unlocked}$ , then `lck` is assigned to one of these threads by

$\xrightarrow{prg}$  in a non-deterministic fashion.  $\xrightarrow{ax}$ ,  $\xrightarrow{prg}$  and the semantic behavior of each statement in PPL are further described below.

To execute a program, or rather, to derive some possible execution trace for a given initial configuration,  $c \in \mathbf{Conf}$ , a succeeding configuration is given by any  $c' \in \mathbf{Conf}$ , such that  $c \xrightarrow{prg} c'$ . Then, a succeeding configuration,  $c'' \in \mathbf{Conf}$ , to  $c'$  is given by  $c' \xrightarrow{prg} c''$ , and so on.

STM( $\mathbf{T}, pc$ )	$\langle pc', r', x', l' \rangle$	If
$[\mathbf{halt}]^{pc}$	$\langle pc, r, x, l \rangle$	
$[\mathbf{skip}]^{pc}$	$\langle pc + 1, r, x, l \rangle$	
$[r := a]^{pc}$	$\langle pc + 1, r[r \mapsto \mathcal{A}[a]r], x, l \rangle$	
$[\mathbf{if } b \mathbf{ goto } l]^{pc}$	$\langle pc + 1, r, x, l \rangle$	$\neg \mathcal{B}[b]r$
$[\mathbf{if } b \mathbf{ goto } l]^{pc}$	$\langle l, r, x, l \rangle$	$\mathcal{B}[b]r$
$[\mathbf{store } r \mathbf{ to } x]^{pc}$	$\langle pc + 1, r, x[x \mapsto (\exists x) \mathbf{T} \mapsto \{(r, t)\}], l \rangle$	
$[\mathbf{load } r \mathbf{ from } x]^{pc}$	$\langle pc + 1, \mathcal{R}(r, r, x, x), x, l \rangle$	
$[\mathbf{lock } lck]^{pc}$	$\langle pc + 1, r, x, l[lck \mapsto (\mathbf{locked}, \mathbf{T}, \mathbf{DL}(\mathbf{l } lck), \mathbf{POWN}(\mathbf{l } lck), \mathbf{REL}(\mathbf{l } lck))] \rangle$	$\mathbf{OWN}(\mathbf{l } lck) = \mathbf{T}$
$[\mathbf{lock } lck]^{pc}$	$\langle pc, r, x, l \rangle$	$\mathbf{OWN}(\mathbf{l } lck) \neq \mathbf{T}$
$[\mathbf{unlock } lck]^{pc}$	$\langle pc + 1, r, x, l[lck \mapsto (\mathbf{unlocked}, \perp_{\mathbf{thrd}}, \mathbf{DL}(\mathbf{l } lck), \mathbf{T}, t)] \rangle$	$\mathbf{OWN}(\mathbf{l } lck) = \mathbf{T}$
$[\mathbf{unlock } lck]^{pc}$	$\langle pc + 1, r, x, l \rangle$	$\mathbf{OWN}(\mathbf{l } lck) \neq \mathbf{T}$
<p>where <math>\mathcal{R}(r, r, x, x) = r[r \mapsto v]</math> for some <math>v</math>, such that</p> $\begin{cases} \exists t' \in \mathbf{Time} : (v, t') \in \bigcup_{T' \in \mathbf{Thrd}} ((\exists x) T') & \mathbf{if } \bigcup_{T' \in \mathbf{Thrd}} ((\exists x) T') \neq \emptyset \\ v \in \gamma_{\mathbf{int}}([-\infty, \infty]) & \mathbf{otherwise} \end{cases}$		

Table 4.2:  $\langle \mathbf{T}, pc, r, x, l, t \rangle \xrightarrow{\text{ax}} \langle pc', r', x', l' \rangle$ , the semantics of concrete axiom transitions.

$\frac{\mathbf{Thrd}_{exe} \neq \emptyset \wedge \forall T \in \mathbf{Thrd}_{exe} : \langle T, pc_T, \mathbb{T}, \mathbb{x}, \mathbb{l}'' , t_T^a \rangle \xrightarrow{ax} \langle pc'_T, \mathbb{T}', \mathbb{x}' , \mathbb{l}' \rangle}{c @ \langle [T, pc_T, \mathbb{T}, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \xrightarrow{prg} c' @ \langle [T, (T \in \mathbf{Thrd}_{exe} ? pc'_T : pc_T), (T \in \mathbf{Thrd}_{exe} ? \mathbb{T}' : \mathbb{T}), t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}' , \mathbb{l}' \rangle}$
<p><b>where</b></p> $t = \min(\{t_T^a + \text{TIME}(c, T) \mid T \in \mathbf{Thrd} \wedge \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}\})$ $\mathbf{Thrd}_{exe} = \{T \in \mathbf{Thrd} \mid t = t_T^a + \text{TIME}(c, T) \wedge \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}\}$ $t_T^a = \begin{cases} t_T^a + \text{TIME}(c, T) & \text{if } T \in \mathbf{Thrd}_{exe} \\ t_T^a & \text{otherwise} \end{cases}$ $\mathbb{x}' x = \begin{cases} \mathbb{x} x & \text{if } \mathbf{Thrd}_x = \emptyset \\ \lambda T \in \mathbf{Thrd}. (T = T' ? (\mathbb{x}'_{T'} x) T' : \emptyset) & \text{otherwise} \end{cases}$ <p style="margin-left: 40px;"><b>where</b> <math>T'</math> is one of the threads in <math>\mathbf{Thrd}_x = \{T \in \mathbf{Thrd}_{exe} \mid \exists r \in \mathbf{Reg}_T : \text{STM}(T, pc_T) = [\text{store } r \text{ to } x]^{pc_T}\}</math></p> $\mathbb{l}'' lck = \begin{cases} (\text{unlocked}, T', t, \text{POWN}(\mathbb{l} lck), \text{REL}(\mathbb{l} lck)) & \text{for some } T' \in \{T \in \mathbf{Thrd}_{exe} \mid \text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T}\}, \\ & \text{if } \{T \in \mathbf{Thrd}_{exe} \mid \text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T}\} \neq \emptyset \wedge \\ & \text{OWN}(\mathbb{l} lck) = \perp_{\text{thrd}} \\ \mathbb{l} lck & \text{otherwise} \end{cases}$ $\mathbb{l}' lck = \begin{cases} \mathbb{l}'_{\text{OWN}(\mathbb{l}'' lck)} lck & \text{if } \text{OWN}(\mathbb{l}'' lck) \in \mathbf{Thrd}_{exe} \\ \mathbb{l} lck & \text{otherwise} \end{cases}$

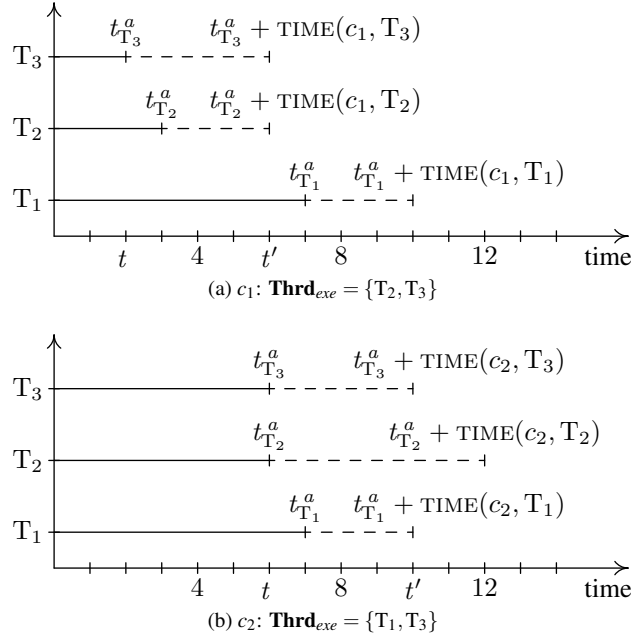
Table 4.3:  $c \xrightarrow{prg} c'$ , the semantics of concrete program transitions.

$STM : (\text{Thrd} \times \text{Lbl}) \rightarrow \text{Stm} = ((\text{ThrdID} \times \text{Stm}) \times \text{Lbl}) \rightarrow \text{Stm}$	$STM((d, s), pc) = \begin{cases} s & \text{if } s = [\text{skip}]^{pc} \vee \\ & s = [r := a]^{pc} \vee \\ & s = [\text{if } b \text{ goto } l']^{pc} \vee \\ & s = [\text{load } r \text{ from } x]^{pc} \vee \\ & s = [\text{store } r \text{ to } x]^{pc} \vee \\ & s = [\text{lock } lck]^{pc} \vee \\ & s = [\text{unlock } lck]^{pc} \vee \\ & s = [\text{halt}]^{pc} \\ STM((d, s'), pc) & \text{if } s = s'; s'' \wedge pc \in \text{LABELS}(s') \\ STM((d, s''), pc) & \text{if } s = s'; s'' \wedge pc \in \text{LABELS}(s'') \end{cases}$
$\text{LABELS} : \text{Stm} \rightarrow \mathcal{P}(\text{Lbl})$	$\text{LABELS}(s) = \begin{cases} \{l\} & \text{if } s = [\text{skip}]^l \vee \\ & s = [r := a]^l \vee \\ & s = [\text{if } b \text{ goto } l']^l \vee \\ & s = [\text{load } r \text{ from } x]^l \vee \\ & s = [\text{store } r \text{ to } x]^l \vee \\ & s = [\text{lock } lck]^l \vee \\ & s = [\text{unlock } lck]^l \vee \\ & s = [\text{halt}]^l \\ \text{LABELS}(s') \cup \text{LABELS}(s'') & \text{if } s = s'; s'' \end{cases}$

Table 4.4: Definition of STM and LABELS.

$\text{STT} : (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time}) \rightarrow \mathbf{Lck}_{\text{stt}}$ $\text{STT}((u, T, t, T', t')) = u$
$\text{OWN} : (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time}) \rightarrow \mathbf{Thrd}_{\perp}$ $\text{OWN}((u, T, t, T', t')) = T$
$\text{DL} : (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time}) \rightarrow \mathbf{Time}$ $\text{DL}((u, T, t, T', t')) = t$
$\text{POWN} : (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time}) \rightarrow \mathbf{Thrd}_{\perp}$ $\text{POWN}((u, T, t, T', t')) = T'$
$\text{REL} : (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time}) \rightarrow \mathbf{Time}$ $\text{REL}((u, T, t, T', t')) = t'$

Table 4.5: Definition of STT, OWN, DL, POWN and REL.


 Figure 4.6: Illustration of how  $\mathbf{Thrd}_{exe}$  is determined ( $c_1 \xrightarrow{prg} c_2$ ).

### TIME and $\mathbf{Thrd}_{exe}$

TIME is assumed to be provided by a timing model of the underlying architecture. It should return a relative execution time for the active statement of thread  $T$ , i.e.,  $\text{STM}(T, pc_T)$ , based on the current system state. Given Assumption 4.1, time is guaranteed to move forward when using  $\xrightarrow{prg}$  for a given configuration (Lemma 4.2). Assumption 4.3 gives that a thread that is waiting to acquire some lock cannot spin an infinite number of times in zero amount of time.

The set of threads to execute,  $\mathbf{Thrd}_{exe}$ , in a given configuration,  $c @ \langle [T, pc_T, \mathbb{R}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{X}, \mathbb{I} \rangle \in \mathbf{Conf}$ , is determined based on  $t_T^a$  and  $\text{TIME}(c, T)$ , for each thread,  $T \in \mathbf{Thrd}$ . It simply consists of the threads that will execute their active statements at the nearest point in time, denoted by  $t$  in Table 4.3. An illustration of how  $\mathbf{Thrd}_{exe}$  is determined is given in Figure 4.6. For  $c_1$  in Figure 4.6a,  $t = t_{T_2}^a + \text{TIME}(c_1, T_2) = t_{T_3}^a + \text{TIME}(c_1, T_3) = 6$  and



$t_{T_1}^a + \text{TIME}(c_1, T_1) = 10$ . Thus,  $\mathbf{Thrd}_{exe} = \{T_2, T_3\}$  and  $t_{T_2}^{a'} = t_{T_3}^{a'} = 6$ , while  $t_{T_1}^{a'} = t_{T_1}^a = 7$ . For  $c_2$  in Figure 4.6b,  $\mathbf{Thrd}_{exe}$  is determined in a similar manner (note that  $c_1 \xrightarrow{prg} c_2$ ).

**Assumption 4.1 (TIME is non-negative):**

It is assumed that  $\forall c \in \mathbf{Conf} : \forall T \in \mathbf{Thrd} : 0 \leq \text{TIME}(c, T)$ .  $\square$

**Lemma 4.2 (Time only moves forward):**

Given that the two configurations  $c @ \langle [T, pc_T, \mathbb{r}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$  and  $c' @ \langle [T, pc'_T, \mathbb{r}'_T, t_T^{a'}]_{T \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf}$  are such that  $c \xrightarrow{prg} c'$ ,  $\forall T \in \mathbf{Thrd} : t_T^a \leq t_T^{a'}$ .  $\square$

PROOF. Assume that  $c @ \langle [T, pc_T, \mathbb{r}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$  and  $c' @ \langle [T, pc'_T, \mathbb{r}'_T, t_T^{a'}]_{T \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf}$  are such that  $c \xrightarrow{prg} c'$ . From Table 4.3, it is apparent that there are two possibilities for the value of  $t_T^{a'}$ .

If  $t_T^a + \text{TIME}(c, T) = \min(\{t_{T'}^a + \text{TIME}(c, T') \mid T' \in \mathbf{Thrd}\}) \wedge \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}$ , then  $t_T^{a'} = t_T^a + \text{TIME}(c, T)$ . Thus,  $t_T^{a'} \geq t_T^a$  (Assumption 4.1).

If  $t_T^a + \text{TIME}(c, T) \neq \min(\{t_{T'}^a + \text{TIME}(c, T') \mid T' \in \mathbf{Thrd}\}) \vee \text{STM}(T, pc_T) = [\text{halt}]^{pc_T}$ , then  $t_T^{a'} = t_T^a$ .

Thus, it must be that  $\forall T \in \mathbf{Thrd} : t_T^a \leq t_T^{a'}$ .  $\blacksquare$

**Assumption 4.3 (TIME is non-zero when spin-locking):**

It is assumed that  $\forall c @ \langle [T, pc_T, \mathbb{r}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf} : \forall T \in \mathbf{Thrd} : ((\exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{OWN}(\mathbb{l} lck) \notin \{\perp_{thrd}, T\})) \Rightarrow 0 < \text{TIME}(c, T))$ .  $\square$

**halt and skip**

As previously discussed, **halt** stops the execution of a thread and **skip** is a no-operation. This is implemented by letting the semantic rule for **halt** return the input state without modifying it, which means that the issuing thread will still be executing the same **halt**-statement in the next iterative step; thus the thread halts. Note that threads issuing a **halt**-statement are not included in  $\mathbf{Thrd}_{exe}$ , however. The rule for the **skip**-statement only increments the thread's program counter,  $pc$ , and thus advances the thread to execute its subsequent statement in the next iterative step.

**:= and  $\mathcal{A}$**

The statement  $r := a$  returns a register state in which the register  $r$  has the value of the arithmetic expression  $a$ . The value of  $a$  is, in the general case,

$$\begin{array}{ll}
\mathcal{A}[[n]]_{\mathbf{r}} = n & \mathcal{A}[[a_1 - a_2]]_{\mathbf{r}} = \mathcal{A}[[a_1]]_{\mathbf{r}} - \mathcal{A}[[a_2]]_{\mathbf{r}} \\
\mathcal{A}[[r]]_{\mathbf{r}} = \mathbf{r} \, r & \mathcal{A}[[a_1 * a_2]]_{\mathbf{r}} = \mathcal{A}[[a_1]]_{\mathbf{r}} \cdot \mathcal{A}[[a_2]]_{\mathbf{r}} \\
\mathcal{A}[[a_1 + a_2]]_{\mathbf{r}} = \mathcal{A}[[a_1]]_{\mathbf{r}} + \mathcal{A}[[a_2]]_{\mathbf{r}} & \mathcal{A}[[a_1 / a_2]]_{\mathbf{r}} = \left\lfloor \frac{\mathcal{A}[[a_1]]_{\mathbf{r}}}{\mathcal{A}[[a_2]]_{\mathbf{r}}} \right\rfloor
\end{array}$$

Table 4.7: Semantics of concrete evaluation of arithmetic expressions.

$$\begin{array}{ll}
\mathcal{B}[[\mathbf{true}]]_{\mathbf{r}} \iff \mathbf{true} & \mathcal{B}[[b_1 \ \&\& \ b_2]]_{\mathbf{r}} \iff \mathcal{B}[[b_1]]_{\mathbf{r}} \wedge \mathcal{B}[[b_2]]_{\mathbf{r}} \\
\mathcal{B}[[\mathbf{false}]]_{\mathbf{r}} \iff \mathbf{false} & \mathcal{B}[[a_1 == a_2]]_{\mathbf{r}} \iff \mathcal{A}[[a_1]]_{\mathbf{r}} = \mathcal{A}[[a_2]]_{\mathbf{r}} \\
\mathcal{B}[[! b]]_{\mathbf{r}} \iff \neg \mathcal{B}[[b]]_{\mathbf{r}} & \mathcal{B}[[a_1 <= a_2]]_{\mathbf{r}} \iff \mathcal{A}[[a_1]]_{\mathbf{r}} \leq \mathcal{A}[[a_2]]_{\mathbf{r}}
\end{array}$$

Table 4.8: Semantics of concrete evaluation of boolean expressions.

dependent on the register values in the input register state and is determined using the function  $\mathcal{A} : \mathbf{Aexp} \rightarrow (\mathbf{Reg} \rightarrow \mathbf{Val}) \rightarrow \mathbf{Val}$ .  $\mathcal{A}$  evaluates arithmetic expressions based on a given register state as defined in Table 4.7.

#### if and $\mathcal{B}$

The statement `if  $b$  goto  $l$`  performs conditional branching. If the boolean expression  $b$  evaluates to `true`, the issuing thread's  $pc$  is set to  $l$ . If  $b$  evaluates to `false`, then `if` acts like the `skip`-statement. The value of  $b$  is, in the general case, dependent on the register values in the input register state and is determined using the function  $\mathcal{B} : \mathbf{Bexp} \rightarrow (\mathbf{Reg} \rightarrow \mathbf{Val}) \rightarrow \mathbf{Bool}$ .  $\mathcal{B}$  evaluates boolean expressions based on a given register state as defined in Table 4.8.

#### store and load

To achieve a high precision in the analysis (see Chapters 5 and 6), the abstraction of the state for variables will need to save write history; i.e., what abstract

writes (each write being a pair of value and time) have been performed by each thread on each variable (see Chapter 5). Therefore, to derive a Galois connection between the concrete and abstract domains for variable states, the concrete state,  $\mathbb{x}$ , has to be defined accordingly. This is why the definition of  $\mathbb{x}$  might look a bit peculiar at first glance. In the concrete semantics, only one single write is saved for each variable, though, since this is all the information that is needed in the concrete case. If several threads write to a variable (using the `store`-statement) at the same time, there is a race on that variable and the resulting state will contain one of the writes; i.e., one of the threads will win the race. The winning thread is non-deterministically chosen from one of the threads writing the variable at the given point in time.

`load` is defined to put the value of the saved write (or rather, the value of one of the saved writes in the general case) in the given register.

#### lock and unlock

As the observant reader might have noticed already, the only information that should be needed in order to successfully express the semantic behavior of locks is what thread is currently assigned (i.e., is currently the owner of) a lock. This is truly the case. However, the extra information given in the concrete state for locks,  $\mathbb{l}$ , will ease the deriving of an approximation of the concrete semantics (see Chapter 5) and achieve a high precision in the analysis (see Chapter 6). This is why the definition of  $\mathbb{l}$  might look a bit peculiar at first glance. Here, the state of locks, i.e., *locked* or *unlocked*, is only used to increase the readability of the rules in Tables 4.2 and 4.3. Note that a consequence of this is that, in a given configuration,  $c@ \langle [T, pc_T, \mathbb{r}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle$ ,  $\text{STT}(\mathbb{l} \text{ lck}) = \textit{locked}$  whenever  $\text{OWN}(\mathbb{l} \text{ lck}) \neq \perp_{\text{thrd}}$  (c.f., Lemma 4.5). Also note that  $(\text{STT}(\mathbb{l} \text{ lck}) = \textit{locked} \wedge \text{OWN}(\mathbb{l} \text{ lck}) = \perp_{\text{thrd}}) \vee \exists T \in \mathbf{Thrd} : t_T^a + \text{TIME}(c, T) < \text{REL}(\mathbb{l} \text{ lck})$  implies that the given configuration is actually not valid (c.f., Definition 4.4).

The `lock`-statement has the same behavior as the `halt`-statement as long as the issuing thread is not assigned the given lock; i.e., the issuing thread will wait for its turn to acquire the lock. If the issuing thread is assigned the given lock (within  $\xrightarrow[\text{prog}]{} \rightarrow$ , using  $\mathbb{l}''$ ), `lock` is defined to basically take the lock (i.e., set its state to *locked*) and advance the thread's `pc`. Only one single thread can be assigned a given lock at any point in time.

The `unlock`-statement has the same behavior as the `skip`-statement if the given lock is not assigned to the issuing thread. If the issuing thread is assigned the given lock, `unlock` is defined to release the lock so that it can be re-assigned in the next iterative step to some thread, if any, issuing `lock` on it.

Note that a thread can repeatedly acquire a lock that is assigned to, and taken by, it, without first releasing it.

**Definition 4.4 (Valid concrete configuration):**

A concrete configuration,  $c @ \langle [\mathbb{T}, pc_{\mathbb{T}}, \mathbb{T}, t_{\mathbb{T}}^a]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$ , is valid with respect to the lock state,  $\mathbb{l}$ , iff

$$\begin{aligned} \forall lck \in \mathbf{Lck} : & ((\text{STT}(\mathbb{l} \ lck) = \text{locked} \Leftrightarrow \text{OWN}(\mathbb{l} \ lck) \neq \perp_{\text{thrd}}) \wedge \\ & (\text{STT}(\mathbb{l} \ lck) = \text{unlocked} \Leftrightarrow \text{OWN}(\mathbb{l} \ lck) = \perp_{\text{thrd}}) \wedge \\ & \forall \mathbb{T} \in \mathbf{Thrd} : \text{REL}(\mathbb{l} \ lck) \leq t_{\mathbb{T}}^a + \text{TIME}(c, \mathbb{T})) \quad \square \end{aligned}$$

**Lemma 4.5 ( $\xrightarrow{\text{prg}}$  preserves lock state validity):**

Given that the configuration  $c @ \langle [\mathbb{T}, pc_{\mathbb{T}}, \mathbb{T}, t_{\mathbb{T}}^a]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$  is valid (c.f., Definition 4.4), then so is  $c' @ \langle [\mathbb{T}, pc'_{\mathbb{T}}, \mathbb{T}, t_{\mathbb{T}}^{a'}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf}$ , whenever  $c \xrightarrow{\text{prg}} c'$ .  $\square$

PROOF. From Table 4.2, it is apparent that the possible axiom output lock states, called  $\mathbb{l}'_{\mathbb{T}}$  in Table 4.3, given an input lock state, called  $\mathbb{l}''$  in Table 4.3, are

1.  $\mathbb{l}''[lck \mapsto (\text{locked}, \mathbb{T}, \text{DL}(\mathbb{l}'' \ lck), \text{POWN}(\mathbb{l}'' \ lck), \text{REL}(\mathbb{l}'' \ lck))]$ , whenever  $\text{STM}(\mathbb{T}, pc_{\mathbb{T}}) = [\text{lock} \ lck]^{pc_{\mathbb{T}}} \wedge \text{OWN}(\mathbb{l}'' \ lck) = \mathbb{T}$ ,
2.  $\mathbb{l}''[lck \mapsto (\text{unlocked}, \perp_{\text{thrd}}, \text{DL}(\mathbb{l}'' \ lck), \mathbb{T}, t_{\mathbb{T}}^{a'})]$ , whenever  $\text{STM}(\mathbb{T}, pc_{\mathbb{T}}) = [\text{unlock} \ lck]^{pc_{\mathbb{T}}} \wedge \text{OWN}(\mathbb{l}'' \ lck) = \mathbb{T}$ , and
3.  $\mathbb{l}''$ , otherwise.

Assume that the configurations  $c @ \langle [\mathbb{T}, pc_{\mathbb{T}}, \mathbb{T}, t_{\mathbb{T}}^a]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$  and  $c' @ \langle [\mathbb{T}, pc'_{\mathbb{T}}, \mathbb{T}, t_{\mathbb{T}}^{a'}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf}$  are such that  $c$  is valid and  $c \xrightarrow{\text{prg}} c'$ .

From Table 4.3, it is apparent that  $\xrightarrow{\text{ax}}$  is only applied to axiom input configurations in which  $\mathbb{l}''$  is such that

1.  $\mathbb{l}'' \ lck = \mathbb{l} \ lck$ , or
2.  $\mathbb{l}'' \ lck = (\text{unlocked}, \mathbb{T}, t_{\mathbb{T}}^{a'}, \text{POWN}(\mathbb{l} \ lck), \text{REL}(\mathbb{l} \ lck))$ .

For the first case, it is easy to see that all the three possible output lock states result in a valid configuration since  $c$  is valid.

The second case only occurs when  $\exists \mathbb{T}' \in \mathbf{Thrd}_{\text{exe}} : (\text{STM}(\mathbb{T}', pc_{\mathbb{T}'}) = [\text{lock} \ lck]^{pc_{\mathbb{T}'}} \wedge \text{OWN}(\mathbb{l} \ lck) = \perp_{\text{thrd}})$ . Note that the assigned owner,

$T \in \mathbf{Thrd}_{exe}$ , is one of the threads executing `lock lck`. For thread  $T$ , the output lock state is  $\mathbb{1}''[lck \mapsto (\text{locked}, T, \text{DL}(\mathbb{1}'' lck), \text{POWN}(\mathbb{1}'' lck), \text{REL}(\mathbb{1}'' lck))]$ , since  $\text{STM}(T, pc_T) = [\text{lock lck}]^{pc_T} \wedge \text{OWN}(\mathbb{1}'' lck) = T$ . Hence,  $\mathbb{1}' lck = \mathbb{1}[lck \mapsto (\text{locked}, T, t_T^a, \text{POWN}(\mathbb{1} lck), \text{REL}(\mathbb{1} lck))]$ .

Since time moves forward for each thread (Lemma 4.2), it is easy to see that  $c'$  is valid.  $\blacksquare$

Lemma 4.6 gives some important properties of the “intermediate” lock state,  $\mathbb{1}''$ , defined in Table 4.3, which is used as a means of assigning a lock to a specific thread. These properties will be used when proving the correctness of the abstract semantics in Tables 5.5 and 5.6.

**Lemma 4.6 (Properties of  $\mathbb{1}''$ ):**

If for some valid configuration,  $c @ \langle [T, pc_T, \mathbb{1}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{1} \rangle \in \mathbf{Conf}$ , and lock,  $lck \in \mathbf{Lck}$ ,  $\text{OWN}(\mathbb{1} lck) = \perp_{thrd} \wedge \exists T' \in \{T \in \mathbf{Thrd}_{exe} \mid \text{STM}(T, pc_T) = [\text{lock lck}]^{pc_T}\} : \text{OWN}(\mathbb{1}'' lck) = T'$ , where  $\mathbb{1}''$  and  $\mathbf{Thrd}_{exe}$  are as defined in Table 4.3, then

1.  $\text{STT}(\mathbb{1}'' lck) = \text{unlocked}$ ,
2.  $\text{DL}(\mathbb{1}'' lck) \not\prec t_{T'}^a$ , and
3.  $t_{T'}^a \not\prec \text{REL}(\mathbb{1}'' lck)$ .  $\square$

**PROOF.** For this proof, each of the properties above will be shown based on the definition of  $\xrightarrow{ax}$  and  $\xrightarrow{prg}$ , defined in Tables 4.2 and 4.3, respectively.

Assume that for the valid configuration  $c @ \langle [T, pc_T, \mathbb{1}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{1} \rangle \in \mathbf{Conf}$  (c.f., Definition 4.4) and some lock,  $lck \in \mathbf{Lck}$ ,  $\text{OWN}(\mathbb{1} lck) = \perp_{thrd} \wedge \exists T' \in \{T \in \mathbf{Thrd}_{exe} \mid \text{STM}(T, pc_T) = [\text{lock lck}]^{pc_T}\} : \text{OWN}(\mathbb{1}'' lck) = T'$ .

1 follows directly from the definition of  $\mathbb{1}''$  in Table 4.3.

Table 4.3 also gives that  $\text{DL}(\mathbb{1}'' lck) = t$  and that  $t_{T'}^a = t$ , since  $T' \in \mathbf{Thrd}_{exe} \wedge \text{STM}(T, pc_T) = [\text{lock lck}]^{pc_T}$ . Thus,  $\text{DL}(\mathbb{1}'' lck) = t_{T'}^a$ , and hence, 2 has been shown.

For 3, Assumption 4.1 gives that time moves forward when using  $\xrightarrow{prg}$  (Lemma 4.2). Thus, it must be that  $t_{T'}^a = t \geq \text{REL}(\mathbb{1} lck) = \text{REL}(\mathbb{1}'' lck)$  (c.f., Table 4.3), which concludes the proof.  $\blacksquare$

### 4.3 Collecting Semantics

This section defines the collecting semantics,  $\mathcal{C}(C)$ , of a program; i.e., the set of all possible semantic configurations given an initial set of configurations,  $C$ , (c.f., Definition 4.7).

**Definition 4.7 (Collecting semantics):**

*The collecting semantics,  $\mathcal{C}(C)$ , of an initial set of configurations,  $C$ , is defined as:*

$$\mathcal{C}(C) = \bigcup_{i \geq 0} C^i \quad \text{where} \quad \begin{cases} C^0 = C \\ C^{i+1} = \{c' \in \mathbf{Conf} \mid \exists c \in C^i : c \xrightarrow{\text{prg}} c'\} \end{cases} \quad \square$$

As can be seen, the collecting semantics will include all possible configurations that a given initial configuration can ever reach. Note that the collecting semantics might be of infinite size in the case of a non-terminating program; i.e., the accumulated time,  $t_T^a$ , for some thread,  $T \in \mathbf{Thrd}$ , could increase indefinitely.

## Chapter 5

# Abstractly Interpreting PPL

In this chapter, the semantics of PPL, defined in Chapter 4, will be abstracted. First it must be decided what parts of the system state to interpret in an abstract way. Abstract states will be crowned with ‘ $\tilde{\phantom{x}}$ ’.

To allow for the hardware timing model to be approximated as well, **Time** will be abstracted using the interval domain, i.e.,  $\mathbf{Time} = \mathbf{Intv}$ . This approach is also taken by Chattopadhyay et al. [11] to approximate the execution time of pipeline stages in order to deal with timing anomalies in multi-core platforms. **Val** will also be abstracted using intervals, i.e.,  $\mathbf{Val} = \mathbf{Intv}$ , to allow for an efficient handling of data flow (note that many other domains could be used as well). Since **Thrd**, **Lbl**, **Var**, **Reg**, **Lck**, **Aexp** and **Bexp** are defined by the software, and the elements of them are used as identifiers, it does not make much sense to abstract them for the defined analysis (see Chapter 6). And, since **Lck<sub>stt</sub>** is comparable to **Bool**, an abstraction of it would most probably not be very beneficial. The states affected by the abstractions of **Time** and **Val** are  $\mathbf{x}$ ,  $\mathbf{x}$ ,  $t^a$ ,  $\mathbf{l}$  and  $\mathbf{c}$ . The abstraction of these will be referred to as  $\tilde{\mathbf{x}}$ ,  $\tilde{\mathbf{x}}$ ,  $\tilde{t}^a$ ,  $\tilde{\mathbf{l}}$  and  $\tilde{\mathbf{c}}$ , respectively.

NOTE. A summary of the notation and nomenclature used in this thesis can be found in Appendix A.

## 5.1 Arithmetical Operators for Intervals

Since values and time are abstracted using the interval domain, the operators of PPL must be extended to act on intervals. This is done in Table 5.1; note that  $\infty/\infty$ ,  $0/0$ ,  $0 * \infty$  and  $\infty - \infty$  need not be defined – they all result in  $[-\infty, \infty]$ .

NOTE. In the following,  $\tilde{+}_t$  and  $\tilde{+}_{val}$  both refer to  $+_{int}$ , and similarly for the rest of the operators.

## 5.2 Abstract Register States

Using Theorems 3.24 and 3.39, it is easy to see that there is indeed a Galois connection,  $\langle \alpha_{reg}, \gamma_{reg} \rangle$ , between the concrete domain  $\mathcal{P}(\mathbf{Reg} \rightarrow \mathbf{Val})$  and the abstract domain  $(\mathbf{Reg} \rightarrow \mathbf{Val}) \cup \{\tilde{\perp}_{reg}, \tilde{\top}_{reg}\}$  (Theorem 5.6). The concretization function,  $\gamma_{reg}$ , partial order,  $\tilde{\subseteq}_{reg}$ , greatest lower bound,  $\tilde{\bigwedge}_{reg}$ , least upper bound,  $\tilde{\bigvee}_{reg}$ , and abstraction function,  $\alpha_{reg}$ , are given by Definitions 5.1, 5.2, 5.3, 5.4 and 5.5, respectively.  $\tilde{\perp}$  is the bottom element,  $\tilde{\perp}_{reg}$ , if  $\exists r \in \mathbf{Reg} : \tilde{\perp} r = \tilde{\perp}_{val}$ ; i.e., if  $\tilde{\perp}$  maps some register to  $\tilde{\perp}_{val}$ . The top element,  $\tilde{\top}_{reg}$ , corresponds to an abstract mapping for which all registers map to  $\tilde{\top}_{val}$ .

**Definition 5.1 (Concretization of an abstract register state):**

$$\gamma_{reg}(\tilde{\pi}) = \begin{cases} \mathbf{Reg} \rightarrow \mathbf{Val} & \text{if } \tilde{\pi} = \tilde{\top}_{reg} \\ \emptyset & \text{if } \tilde{\pi} = \tilde{\perp}_{reg} \\ \{\lambda r \in \mathbf{Reg}. v \mid v \in \gamma_{val}(\tilde{\pi} r)\} & \text{otherwise} \end{cases} \quad \square$$

**Definition 5.2 (Partial order for abstract register states):**

$$\begin{cases} \tilde{\pi} \tilde{\subseteq}_{reg} \tilde{\top}_{reg} \\ \tilde{\perp}_{reg} \tilde{\subseteq}_{reg} \tilde{\pi} \\ \tilde{\pi} \tilde{\subseteq}_{reg} \tilde{\pi}' \iff \forall r \in \mathbf{Reg} : \tilde{\pi} r \tilde{\subseteq}_{val} \tilde{\pi}' r \end{cases} \quad \square$$



$\top_{int} op_{int} i = i op_{int} \top_{int} = \top_{int}$ $\perp_{int} op_{int} i = i op_{int} \perp_{int} = \perp_{int}$		<b>where</b> $op_{int} \in \{+_{int}, -_{int}, *__{int}, /_{int}\}$
$[n_1, n_2] +_{int} [n'_1, n'_2]$	$= \begin{cases} [n_1 + n'_1, n_2 + n'_2] & \text{if } -\infty < n_1, n'_1, n_2, n'_2 < \infty \\ [n_1 + n'_1, \infty] & \text{if } (n_2 = \infty \vee n'_2 = \infty) \wedge \\ & \neg((n_1 = -\infty \wedge n'_1 = \infty) \vee \\ & (n_1 = \infty \wedge n'_1 = -\infty)) \\ [-\infty, n_2 + n'_2] & \text{if } (n_1 = -\infty \vee n'_1 = -\infty) \wedge \\ & \neg((n_2 = -\infty \wedge n'_2 = \infty) \vee \\ & (n_2 = \infty \wedge n'_2 = -\infty)) \\ [-\infty, \infty] & \text{otherwise} \end{cases}$	
$[n_1, n_2] -_{int} [n'_1, n'_2]$	$= \begin{cases} [n_1 - n'_2, n_2 - n'_1] & \text{if } -\infty < n_1, n'_1, n_2, n'_2 < \infty \\ [n_1 - n'_2, \infty] & \text{if } (n_2 = \infty \vee n'_1 = -\infty) \wedge \\ & \neg((n_1 = \infty \wedge n'_2 = \infty) \vee \\ & (n_1 = -\infty \wedge n'_2 = -\infty)) \\ [-\infty, n_2 - n'_1] & \text{if } (n_1 = -\infty \vee n'_2 = \infty) \wedge \\ & \neg((n_2 = \infty \wedge n'_1 = \infty) \vee \\ & (n_2 = -\infty \wedge n'_1 = -\infty)) \\ [-\infty, \infty] & \text{otherwise} \end{cases}$	
$[n_1, n_2] *__{int} [n'_1, n'_2]$	$= \begin{cases} [\min(V), \max(V)] & \text{if } (n_2 < 0 \wedge n'_1 > 0) \vee \\ & (n_2 < 0 \wedge n'_2 < 0) \vee \\ & (n_1 > 0 \wedge n'_1 > 0) \vee \\ & (n_1 > 0 \wedge n'_2 < 0) \vee \\ & (-\infty < n_1, n'_1, n_2, n'_2 < \infty) \\ [-\infty, \infty] & \text{otherwise} \end{cases}$ <p style="text-align: center;"><b>where</b> <math>V = \{n_1 * n'_1, n_1 * n'_2, n_2 * n'_1, n_2 * n'_2\}</math></p>	
$[n_1, n_2] /_{int} [n'_1, n'_2]$	$= \begin{cases} [[\min(V)], [\max(V)]] & \text{if } (-\infty < n'_1 \wedge n'_2 < 0) \vee \\ & (0 < n'_1 \wedge n'_2 < \infty) \\ [-\infty, -n_1] & \text{if } n'_1 \leq 0 \leq n'_2 \wedge n_2 < 0 \\ [-n_2, \infty] & \text{if } n'_1 \leq 0 \leq n'_2 \wedge 0 < n_1 \\ [-\infty, \infty] & \text{otherwise} \end{cases}$ <p style="text-align: center;"><b>where</b> <math>V = \{n_1/n'_1, n_1/n'_2, n_2/n'_1, n_2/n'_2\}</math></p>	

Table 5.1: PPL operators defined for interval arguments.

**Definition 5.3 (Greatest lower bound of abstract register states):**

$$\begin{cases} \tilde{\top}_{reg} \sqcap_{reg} \tilde{\mathbb{I}} = \tilde{\mathbb{I}} \sqcap_{reg} \tilde{\top}_{reg} = \tilde{\mathbb{I}} \\ \tilde{\perp}_{reg} \sqcap_{reg} \tilde{\mathbb{I}} = \tilde{\mathbb{I}} \sqcap_{reg} \tilde{\perp}_{reg} = \tilde{\perp}_{reg} \\ (\tilde{\mathbb{I}} \sqcap_{reg} \tilde{\mathbb{I}}') r = (\tilde{\mathbb{I}} r) \sqcap_{val} (\tilde{\mathbb{I}}' r) \end{cases} \quad \square$$

**Definition 5.4 (Least upper bound of abstract register states):**

$$\begin{cases} \tilde{\top}_{reg} \sqcup_{reg} \tilde{\mathbb{I}} = \tilde{\mathbb{I}} \sqcup_{reg} \tilde{\top}_{reg} = \tilde{\top}_{reg} \\ \tilde{\perp}_{reg} \sqcup_{reg} \tilde{\mathbb{I}} = \tilde{\mathbb{I}} \sqcup_{reg} \tilde{\perp}_{reg} = \tilde{\mathbb{I}} \\ (\tilde{\mathbb{I}} \sqcup_{reg} \tilde{\mathbb{I}}') r = (\tilde{\mathbb{I}} r) \sqcup_{val} (\tilde{\mathbb{I}}' r) \end{cases} \quad \square$$

**Definition 5.5 (Abstraction of a set of register states):**

$$\alpha_{reg}(\mathbb{R}) = \begin{cases} \tilde{\top}_{reg} & \text{if } \mathbb{R} = \mathbf{Reg} \rightarrow \mathbf{Val} \\ \tilde{\perp}_{reg} & \text{if } \mathbb{R} = \emptyset \\ \lambda r \in \mathbf{Reg}. \alpha_{val}(\{\mathbb{I} r \mid \mathbb{I} \in \mathbb{R}\}) & \text{otherwise} \end{cases} \quad \square$$

**Theorem 5.6 (Galois connection – Register states):**

$\langle \alpha_{reg}, \gamma_{reg} \rangle$ , where  $\gamma_{reg}$  and  $\alpha_{reg}$  are defined as in Definitions 5.1 and 5.5, respectively, is a Galois connection.  $\square$

PROOF. Since  $\alpha_{val} = \alpha_{int}$  and  $\gamma_{val} = \gamma_{int}$ ,  $\langle \alpha_{val}, \gamma_{val} \rangle$  is a Galois insertion between  $\mathcal{P}(\mathbf{Val})$  and  $\mathbf{V\tilde{a}l}$  (Theorem 3.39).

By Theorem 3.24,  $\langle \alpha_{reg} : \mathcal{P}(\mathbf{Reg} \rightarrow \mathbf{Val}) \rightarrow ((\mathbf{Reg} \rightarrow \mathbf{V\tilde{a}l}) \cup \{\tilde{\perp}_{reg}, \tilde{\top}_{reg}\}), \gamma_{reg} : ((\mathbf{Reg} \rightarrow \mathbf{V\tilde{a}l}) \cup \{\tilde{\perp}_{reg}, \tilde{\top}_{reg}\}) \rightarrow \mathcal{P}(\mathbf{Reg} \rightarrow \mathbf{Val}) \rangle$ , where  $\gamma_{reg}$  and  $\alpha_{reg}$  are as presented in Definitions 5.1 and 5.5, respectively, is a Galois connection.  $\blacksquare$

### 5.3 Abstract Evaluation of Arithmetical Expressions

The function evaluating arithmetic expressions,  $\mathcal{A}$ , must be abstracted since values and register states are abstracted. The abstraction will be  $\tilde{\mathcal{A}} : \mathbf{Aexp} \rightarrow (\mathbf{Reg} \rightarrow \mathbf{V\tilde{a}l}) \rightarrow \mathbf{V\tilde{a}l}$ , which is equivalent to  $\tilde{\mathcal{A}} : \mathbf{Aexp} \rightarrow (\mathbf{Reg} \rightarrow \mathbf{Intv}) \rightarrow$

$\mathcal{A}[[n]]\tilde{r} = \alpha_{val}(\{n\})$	$\mathcal{A}[[a_1 + a_2]]\tilde{r} = \mathcal{A}[[a_1]]\tilde{r} \dot{+}_{val} \mathcal{A}[[a_2]]\tilde{r}$
$\mathcal{A}[[r]]\tilde{r} = \tilde{r} r$	$\mathcal{A}[[a_1 - a_2]]\tilde{r} = \mathcal{A}[[a_1]]\tilde{r} \dot{-}_{val} \mathcal{A}[[a_2]]\tilde{r}$
	$\mathcal{A}[[a_1 * a_2]]\tilde{r} = \mathcal{A}[[a_1]]\tilde{r} \dot{*}_{val} \mathcal{A}[[a_2]]\tilde{r}$
	$\mathcal{A}[[a_1 / a_2]]\tilde{r} = \mathcal{A}[[a_1]]\tilde{r} \dot{/}_{val} \mathcal{A}[[a_2]]\tilde{r}$

Table 5.2: The abstract function evaluating arithmetic expressions.

**Intv**, and can be derived using Definition 3.11 to induce  $\mathcal{A}$ . To do this,  $\mathcal{A}$  must first be lifted to sets of concrete register mappings:

$$\mathcal{A}_{\mathcal{P}}[[a]]\mathbb{R} = \{\mathcal{A}[[a]]r \mid r \in \mathbb{R}\}$$

The abstract evaluation function can then be derived as:

$$\tilde{\mathcal{A}}[[a]] = \alpha_{val} \circ \mathcal{A}_{\mathcal{P}}[[a]] \circ \gamma_{reg}$$

The details of this function can be found in Table 5.2.

## 5.4 Boolean Restriction

The function  $\tilde{\mathcal{B}}_{\mathcal{R}}$ , defined in Definition 5.7, will be used in the abstract axiom transition rules (see Table 5.5 on page 84). This function is safely induced from  $\mathcal{B}$ , using Definition 3.11, so that the concretization of  $\tilde{\mathcal{B}}_{\mathcal{R}}[[b]]\tilde{r}$ , where  $b \in \mathbf{Bexp}$ , always contains (at least) the concrete register states, derived from  $\tilde{r}$ , for which  $b$  evaluates to true.

**Definition 5.7 (Boolean restriction):**

$$\tilde{\mathcal{B}}_{\mathcal{R}}[[b]]\tilde{r} = \alpha_{reg}(\{r \in \gamma_{reg}(\tilde{r}) \mid \mathcal{B}[[b]]r\}) \quad \square$$



**Theorem 5.10 (Galois connection – Variable states):**

$\langle \alpha_{var}, \gamma_{var} \rangle$ , where  $\gamma_{var}$  and  $\alpha_{var}$  are defined as in Definitions 5.8 and 5.9, respectively, defines a Galois connection.

PROOF. Since  $\langle \alpha_{int}, \gamma_{int} \rangle$  is a Galois insertion (Theorem 3.39) and thus a Galois connection, so are  $\langle \alpha_{val}, \gamma_{val} \rangle$  and  $\langle \alpha_t, \gamma_t \rangle$  (since  $\alpha_{val} = \alpha_t = \alpha_{int}$  and  $\gamma_{val} = \gamma_t = \gamma_{int}$ ). Using Theorems 3.17, 3.20 and 3.24 to derive  $\alpha_{var}$  and  $\gamma_{var}$ , the result follows (note that the cases  $\gamma_{var}(\tilde{\top}_{var})$ ,  $\gamma_{var}(\tilde{\perp}_{var})$ ,  $\alpha_{var}(\mathbf{Var} \rightarrow \mathbf{Thrd} \rightarrow (\mathbf{Val} \times \mathbf{Time}))$  and  $\alpha_{var}(\emptyset)$  follow trivially):

$$\begin{aligned} \gamma_{var}(\tilde{x}) &\stackrel{Th. 3.24}{=} \{\lambda x \in \mathbf{Var}.f \mid f \in \gamma'(\tilde{x} \ x)\} \\ &\stackrel{Th. 3.24}{=} \{\lambda x \in \mathbf{Var}.f \mid f \in \{\lambda T \in \mathbf{Thrd}.W \mid W \in \gamma''((\tilde{x} \ x) \ T)\}\} \\ &\stackrel{Th. 3.20}{=} \{\lambda x \in \mathbf{Var}.f \mid f \in \{\lambda T \in \mathbf{Thrd}.W \mid W \in \\ &\qquad\qquad\qquad \{W' \mid \alpha'''(W') \in ((\tilde{x} \ x) \ T)\}\}\} \\ &\stackrel{Th. 3.17}{=} \{\lambda x \in \mathbf{Var}.f \mid f \in \{\lambda T \in \mathbf{Thrd}.W \mid W \in \\ &\qquad\qquad\qquad \{W' \mid (\alpha_{val}(\{v \in \mathbf{Val} \mid \exists t \in \mathbf{Time} : (v, t) \in W'\}), \\ &\qquad\qquad\qquad \alpha_t(\{t \in \mathbf{Time} \mid \exists v \in \mathbf{Val} : (v, t) \in W'\})) \in \\ &\qquad\qquad\qquad ((\tilde{x} \ x) \ T)\}\}\}\} \end{aligned}$$

$$\begin{aligned} \alpha_{var}(\tilde{x}) &\stackrel{Th. 3.24}{=} \lambda x \in \mathbf{Var}.\alpha'(\{\tilde{x} \ x \mid \tilde{x} \in \mathbb{X}\}) \\ &\stackrel{Th. 3.24}{=} \lambda x \in \mathbf{Var}.\lambda T \in \mathbf{Thrd}.\alpha''(\{f \ T \mid f \in \{\tilde{x} \ x \mid \tilde{x} \in \mathbb{X}\}\}) \\ &\stackrel{calc.}{=} \lambda x \in \mathbf{Var}.\lambda T \in \mathbf{Thrd}.\alpha''(\{(\tilde{x} \ x) \ T \mid \tilde{x} \in \mathbb{X}\}) \\ &\stackrel{Th. 3.20}{=} \lambda x \in \mathbf{Var}.\lambda T \in \mathbf{Thrd}.\{\alpha'''(W) \mid W \in \{(\tilde{x} \ x) \ T \mid \tilde{x} \in \mathbb{X}\}\} \\ &\stackrel{Th. 3.17}{=} \lambda x \in \mathbf{Var}.\lambda T \in \mathbf{Thrd}.\{(\alpha_{val}(\{v \mid \exists t \in \mathbf{Time} : (v, t) \in W\}), \\ &\qquad\qquad\qquad \alpha_t(\{t \mid \exists v \in \mathbf{Val} : (v, t) \in W\})) \mid \\ &\qquad\qquad\qquad W \in \{(\tilde{x} \ x) \ T \mid \tilde{x} \in \mathbb{X}\}\} \end{aligned}$$

■

The state  $\tilde{x} \in (\mathbf{Var} \rightarrow \mathbf{Thrd} \rightarrow \mathcal{P}(\mathbf{Val} \times \mathbf{Time})) \cup \{\tilde{\perp}_{var}, \tilde{\top}_{var}\}$  can save any number (i.e., history) of abstract writes,  $\tilde{w} \in \mathbf{Val} \times \mathbf{Time}$ , for each thread that occur on some variable. This is done to counteract the precision loss due to approximating points in time with intervals. The information available in such history makes it possible to use sequence information (within each thread) and timing information (between threads) to get a reasonably tight value when reading a variable.

For convenience in expressing, and increased readability of, the upcoming algorithms, some relations for abstract writes,  $\tilde{w} ::= (\tilde{v}, \tilde{t})$ , will be defined. The

partial order,  $\tilde{\sqsubseteq}_w$ , and least upper bound operator,  $\tilde{\sqcup}_w$ , for writes follow naturally (c.f., Definitions 3.26 and 3.28) from the partial orders and least upper bound operators for values,  $\tilde{\sqsubseteq}_{val}$  and  $\tilde{\sqcup}_{val}$ , and time,  $\tilde{\sqsubseteq}_t$  and  $\tilde{\sqcup}_t$ .  $\tilde{\sqsubseteq}_w$  and  $\tilde{\sqcup}_w$  are given by Definitions 5.11 and 5.12, respectively.

NOTE. The notations “ $\tilde{w}$ ” and “ $(\tilde{v}, \tilde{t})$ ” for abstract writes will from here on be used interchangeably.

**Definition 5.11 (Partial order of writes,  $\tilde{\sqsubseteq}_w$ ):**

$$\begin{cases} \tilde{w} \tilde{\sqsubseteq}_w \tilde{T}_w \\ \tilde{\perp}_w \tilde{\sqsubseteq}_w \tilde{w} \\ (\tilde{v}_1, \tilde{t}_1) \tilde{\sqsubseteq}_w (\tilde{v}_2, \tilde{t}_2) \iff \tilde{v}_1 \tilde{\sqsubseteq}_{val} \tilde{v}_2 \wedge \tilde{t}_1 \tilde{\sqsubseteq}_t \tilde{t}_2 \end{cases} \quad \square$$

**Definition 5.12 (Least upper bound of writes,  $\tilde{\sqcup}_w$ ):**

$$\begin{cases} \tilde{w} \tilde{\sqcup}_w \tilde{T}_w = \tilde{T}_w \tilde{\sqcup}_w \tilde{w} = \tilde{T}_w \\ \tilde{\perp}_w \tilde{\sqcup}_w \tilde{w} = \tilde{w} \tilde{\sqcup}_w \tilde{\perp}_w = \tilde{w} \\ (\tilde{v}_1, \tilde{t}_1) \tilde{\sqcup}_w (\tilde{v}_2, \tilde{t}_2) = (\tilde{v}_1 \tilde{\sqcup}_{val} \tilde{v}_2, \tilde{t}_1 \tilde{\sqcup}_t \tilde{t}_2) \end{cases} \quad \square$$

The precedence relation,  $\tilde{<}_t$ , on abstract times given by Definition 5.13 will be useful to determine whether two writes are performed at disjoint times, or the order two arbitrary events.

**Definition 5.13 (Time precedence,  $\tilde{<}_t$ ):**

$$\begin{cases} \tilde{t} \tilde{<}_t \tilde{T}_t & \text{if } \tilde{t} \neq \tilde{T}_t \\ \tilde{\perp}_t \tilde{<}_t \tilde{t} & \text{if } \tilde{t} \neq \tilde{\perp}_t \\ \tilde{t}_1 \tilde{<}_t \tilde{t}_2 \iff \max(\gamma_t(\tilde{t}_1)) < \min(\gamma_t(\tilde{t}_2)) & \text{if } \tilde{t}_1, \tilde{t}_2 \notin \{\tilde{\perp}_t, \tilde{T}_t\} \end{cases} \quad \square$$

The definitions of  $\tilde{\sqsubseteq}_{var}$ ,  $\tilde{\sqcap}_{var}$  and  $\tilde{\sqcup}_{var}$  follow naturally from the definition of the domain (c.f., Definitions 3.26, 3.27 and 3.28) and are presented in Definitions 5.14, 5.15 and 5.16, respectively. However, these relations and operators cannot be used directly within the analysis to, e.g., join (merge) the histories of writes in several variable states. This is due to the fact that the history in the states might have different sequence information (i.e., traces), that would

be lost if merging the two states. Reading a safe and tight value for a variable requires the sequence information to be available. Therefore, the operations to be used within the analysis should instead be defined based on Definition 5.18 to ensure that all threads see safe values (see Definition 5.19) at all times. Note that Definition 5.17 defines the uniquely most recent write in a set of writes. This definition defines the most recent write both among several threads (globally) and for single threads (locally).

**Definition 5.14 (Partial order for abstract variable states):**

$$\left\{ \begin{array}{l} \tilde{\mathfrak{x}} \sqsubseteq_{var} \tilde{\mathfrak{T}}_{var} \\ \tilde{\mathfrak{T}}_{var} \sqsubseteq_{var} \tilde{\mathfrak{x}} \\ \tilde{\mathfrak{x}} \sqsubseteq_{var} \tilde{\mathfrak{x}}' \iff \forall x \in \mathbf{Var} : \forall T \in \mathbf{Thrd} : (\tilde{\mathfrak{x}} x) T \subseteq (\tilde{\mathfrak{x}}' x) T \end{array} \right. \quad \square$$

**Definition 5.15 (Greatest lower bound of abstract variable states):**

$$\left\{ \begin{array}{l} \tilde{\mathfrak{T}}_{var} \hat{\cap}_{var} \tilde{\mathfrak{x}} = \tilde{\mathfrak{x}} \hat{\cap}_{var} \tilde{\mathfrak{T}}_{var} = \tilde{\mathfrak{x}} \\ \tilde{\mathfrak{T}}_{var} \hat{\cap}_{var} \tilde{\mathfrak{x}} = \tilde{\mathfrak{x}} \hat{\cap}_{var} \tilde{\mathfrak{T}}_{var} = \tilde{\mathfrak{T}}_{var} \\ (((\tilde{\mathfrak{x}} \hat{\cap}_{var} \tilde{\mathfrak{x}}') x) T) = ((\tilde{\mathfrak{x}} x) T) \cap ((\tilde{\mathfrak{x}}' x) T) \end{array} \right. \quad \square$$

**Definition 5.16 (Least upper bound of abstract variable states):**

$$\left\{ \begin{array}{l} \tilde{\mathfrak{T}}_{var} \hat{\sqcup}_{var} \tilde{\mathfrak{x}} = \tilde{\mathfrak{x}} \hat{\sqcup}_{var} \tilde{\mathfrak{T}}_{var} = \tilde{\mathfrak{T}}_{var} \\ \tilde{\mathfrak{T}}_{var} \hat{\sqcup}_{var} \tilde{\mathfrak{x}} = \tilde{\mathfrak{x}} \hat{\sqcup}_{var} \tilde{\mathfrak{T}}_{var} = \tilde{\mathfrak{x}} \\ (((\tilde{\mathfrak{x}} \hat{\sqcup}_{var} \tilde{\mathfrak{x}}') x) T) = ((\tilde{\mathfrak{x}} x) T) \cup ((\tilde{\mathfrak{x}}' x) T) \end{array} \right. \quad \square$$

**Definition 5.17 (Time of most recent write):**

The most recent write(s),  $(\tilde{v}, \tilde{t})$ , in a set of writes is defined such that  $\min(\gamma_t(\tilde{t})) \geq \min(\gamma_t(\tilde{t}'))$ , for all other writes,  $(\tilde{v}', \tilde{t}')$ . If several writes,  $(\tilde{v}', \tilde{t}')$ , are such that  $\min(\gamma_t(\tilde{t})) = \min(\gamma_t(\tilde{t}'))$ , the time of the most recent write,  $\tilde{t}$ , is uniquely determined from the write(s) with  $\max(\gamma_t(\tilde{t})) = \max(\{\max(\gamma_t(\tilde{t}')) \mid \tilde{t}' \text{ ranges over the time-stamps of the writes such that } \min(\gamma_t(\tilde{t})) = \min(\gamma_t(\tilde{t}'))\})$ .  $\square$

NOTE. The definition of the “time of the most recent write” and many of the upcoming algorithms could be very much simplified if the notion of lists were known. The positions of the writes in a list could simply correspond to the sequential order in which they occurred within a thread. Therefore, implementations of the upcoming algorithms could look very different from how they are defined here.

**Definition 5.18 (Safe write history):**

An abstract variable state,  $\tilde{x}$ , is safe at time  $\tilde{t}$  if  $\gamma_{var}(\tilde{x})$  represents at least all the possible concrete variable states that can be valid at time  $t \in \gamma_t(\tilde{t})$  for the given thread trace(s).

Thus, to be safe at time  $\tilde{t}$ ,  $\tilde{x}$  must, for each variable,  $x \in \mathbf{Var}$  and each thread,  $T \in \mathbf{Thrd}$ , be such that  $((\tilde{x} x) T)$  contains at least

1. all writes,  $(\tilde{v}, \tilde{t}')$ , by  $T$  on  $x$ , such that  $\tilde{t}' \not\prec_t \tilde{t} \wedge \tilde{t}' \not\prec_t \tilde{t}$ , and
2. the latest (most recent) write(s),  $(\tilde{v}, \tilde{t}')$ , by  $T$  on  $x$ , such that  $\tilde{t}' \prec_t \tilde{t}$ , if  $\tilde{t}' \not\prec_t \tilde{t}^{mrw} \neq \perp_t$ , where  $\tilde{t}^{mrw}$  is the time of the globally most recent write,

or,

3.  $(\tilde{\perp}_{val}, \tilde{\perp}_t)$ , otherwise (i.e., if there are no writes that fit 1 or 2 above), or if no writes have occurred by  $T$  on  $x$ .

From how the concrete and abstract domains (c.f., Section 4.1 and this section) and transition rules (c.f., Section 4.2) are defined, it is apparent that  $\tilde{x}$  is a safe approximation of  $x$  (i.e.,  $\tilde{x}$  contains safe write history) iff  $\exists x' \in \gamma_{var}(\tilde{x}) : \forall x \in \mathbf{Var} : \forall T \in \mathbf{Thrd} : ((x x) T) \subseteq ((x' x) T)$ .  $\square$

**Definition 5.19 (Safe value of  $x$  as seen by thread  $T$ ):**

Assuming that  $\tilde{x}$  contains safe write history for all threads on variable  $x$ , according to Definition 5.18, then a safe value of  $x$ , as seen by thread  $T$ , at time  $\tilde{t}$  is the least upper bound,  $\tilde{\perp}_{val}$ , of the values of at least the following writes on  $x$ .

1. All writes,  $\tilde{w}_{T'} = (\tilde{v}_{T'}, \tilde{t}_{T'})$ , for threads  $T' \in \mathbf{Thrd} \setminus \{T\}$  on  $x$  such that  $\tilde{t}_{T'} \not\prec_t \tilde{t} \wedge \tilde{t}' \not\prec_t \tilde{t}$ .
2. The most recent write in  $\{(\tilde{v}'_{T'}, \tilde{t}'_{T'}) \in (\tilde{x} x) T' \mid \tilde{t}'_{T'} \prec_t \tilde{t} \wedge \tilde{t}'_{T'} \not\prec_t \tilde{t}^{mrw} \neq \perp_t\}$  for each thread  $T' \in \mathbf{Thrd} \setminus \{T\}$ , and the most recent



write,  $(\tilde{v}'_T, \tilde{t}'_T) \in (\tilde{x} \ x) \ T$ , such that  $\min(\gamma_t(\tilde{t}'_T)) \leq \min(\gamma_t(\tilde{t}))$ , if  $\tilde{t}'_T \hat{r}_t$ ,  $\tilde{t}^{mrw} \neq \perp_t$ , where  $\tilde{t}^{mrw}$  is the time of the (globally) most recent write in  $\{(\tilde{v}'_T, \tilde{t}'_T)\} \cup \bigcup_{T' \in \text{Thrd} \setminus \{T\}} \{(\tilde{v}'_{T'}, \tilde{t}'_{T'}) \in (\tilde{x} \ x) \ T' \mid \tilde{t}'_{T'} \prec_t \tilde{t}\}$ .  $\square$

---

**Algorithm 5.1** Partial Order of Abstract Variable States
 

---

```

1: function PARTIALORDERVAR( $\tilde{x}, \tilde{x}'$ )
2:   for all  $x \in \text{Var}$  do
3:     for all  $T \in \text{Thrd}$  do
4:        $\tilde{W} \leftarrow ((\tilde{x} \ x) \ T)$ 
5:        $\tilde{W}' \leftarrow ((\tilde{x}' \ x) \ T)$ 
6:       while  $\tilde{W} \neq \emptyset \wedge \tilde{W}' \neq \emptyset$  do
7:          $\tilde{w} \leftarrow \text{EARLIESTWRITETHREAD}(\tilde{W})$ 
8:          $\tilde{w}' \leftarrow \text{EARLIESTWRITETHREAD}(\tilde{W}')$ 
9:          $\tilde{W} \leftarrow \tilde{W} \setminus \{\tilde{w}\}$ 
10:         $\tilde{W}' \leftarrow \tilde{W}' \setminus \{\tilde{w}'\}$ 
11:        if  $\tilde{w} \neq \tilde{w}'$  then
12:          if  $\tilde{W}' = \emptyset$  then
13:            for all  $\tilde{w}'' \in \tilde{W} \cup \{\tilde{w}\}$  do
14:              if  $\tilde{w}'' \tilde{\zeta}_w \tilde{w}'$  then
15:                return false
16:              end if
17:            end for
18:             $\tilde{W} \leftarrow \emptyset$ 
19:          else
20:            return false
21:          end if
22:        end if
23:      end while
24:      if  $\tilde{W} \neq \emptyset$  then
25:        return false
26:      end if
27:    end for
28:  end for
29:  return true
30: end function

```

---

The partial order for abstract variable states to be used within the analysis,  $\tilde{\sqsubseteq}'_{var}$ , is given by Definition 5.20 based on PARTIALORDERVAR, defined in Algorithm 5.1, taking the safety of write history (Definition 5.18) into account. Note that EARLIESTWRITETHREAD, as defined in Algorithm 5.2, returns a

---

**Algorithm 5.2** Earliest Write for a Thread

---

```
1: function EARLIESTWRITETHREAD( $\tilde{W}$ )
2:   if  $\tilde{W} = \emptyset$  then
3:     return  $\perp_w$ 
4:   end if
5:    $\tilde{t}_{min} \leftarrow \alpha_t(\{\infty\})$ 
6:   for all  $(\tilde{v}, \tilde{t}) \in \tilde{W}$  do
7:     if  $\min(\gamma_t(\tilde{t})) < \min(\gamma_t(\tilde{t}_{min}))$  then
8:        $\tilde{t}_{min} \leftarrow \tilde{t}$ 
9:     else if  $\min(\gamma_t(\tilde{t})) = \min(\gamma_t(\tilde{t}_{min}))$  then
10:       $\tilde{t}_{min} \leftarrow \tilde{t} \sqcap_t \tilde{t}_{min}$ 
11:    end if
12:  end for
13:   $\tilde{W}' \leftarrow \{(\tilde{v}, \tilde{t}) \mid (\tilde{v}, \tilde{t}) \in \tilde{W} \wedge \tilde{t} = \tilde{t}_{min}\}$ 
14:   $\tilde{v}_{min} \leftarrow \alpha_{val}(\{\infty\})$ 
15:  for all  $(\tilde{v}, \tilde{t}) \in \tilde{W}'$  do
16:    if  $\min(\gamma_{val}(\tilde{v})) < \min(\gamma_{val}(\tilde{v}_{min}))$  then
17:       $\tilde{v}_{min} \leftarrow \tilde{v}$ 
18:    else if  $\min(\gamma_{val}(\tilde{v})) = \min(\gamma_{val}(\tilde{v}_{min}))$  then
19:       $\tilde{v}_{min} \leftarrow \tilde{v} \sqcap_{val} \tilde{v}_{min}$ 
20:    end if
21:  end for
22:  return  $(\tilde{v}_{min}, \tilde{t}_{min})$ 
23: end function
```

---

deterministically defined write. The idea is that the history (trace) for each thread and variable should be the same in both states for the relation to be true. However, the histories are allowed to differ somewhat. The greater state could also contain newer writes than those in the history of the lesser state. It could also be the case that the newest write in the greater state is an upper bound to all of the most recent writes in the lesser state that are not part of both histories.

**Definition 5.20 (Safe partial order of abstract variable states):**

$$\begin{cases} \tilde{x} \sqsubseteq_{var}' \tilde{x}' \\ \tilde{\perp}_{var} \sqsubseteq_{var}' \tilde{x} \\ \tilde{x} \sqsubseteq_{var}' \tilde{x}' \iff \text{PARTIALORDERVAR}(\tilde{x}, \tilde{x}') \end{cases} \quad \square$$

Based on this partial order relation, the lower bound and upper bound operators to be used within the analysis,  $\tilde{\sqcap}'_{var}$  and  $\tilde{\sqcup}'_{var}$ , are given by Definitions 5.21 and 5.22, respectively. Note that MEETVAR is defined in Algorithm 5.3 and JOINVAR is defined in Algorithm 5.4.

**Definition 5.21 (Safe lower bound of abstract variable states):**

$$\begin{cases} \tilde{\sqcap}'_{var} \tilde{x} = \tilde{x} \cap'_{var} \tilde{\perp}_{var} = \tilde{x} \\ \tilde{\sqcap}'_{var} \tilde{\perp}_{var} = \tilde{\perp}_{var} \cap'_{var} \tilde{x} = \tilde{\perp}_{var} \\ \tilde{x} \cap'_{var} \tilde{x}' = \text{MEETVAR}(\tilde{x}, \tilde{x}') \end{cases} \quad \square$$

**Definition 5.22 (Safe upper bound of abstract variable states):**

$$\begin{cases} \tilde{\sqcup}'_{var} \tilde{x} = \tilde{x} \sqcup'_{var} \tilde{\perp}_{var} = \tilde{\sqcup}'_{var} \\ \tilde{\sqcup}'_{var} \tilde{\perp}_{var} = \tilde{\perp}_{var} \sqcup'_{var} \tilde{x} = \tilde{\sqcup}'_{var} \\ \tilde{x} \sqcup'_{var} \tilde{x}' = \text{JOINVAR}(\tilde{x}, \tilde{x}') \end{cases} \quad \square$$

NOTE. Neither  $\tilde{\sqsubseteq}'_{var}$ ,  $\tilde{\sqcap}'_{var}$  nor  $\tilde{\sqcup}'_{var}$  is currently used by the analysis (c.f., Chapter 6) but are just presented for completeness of the abstraction since the operators cannot be directly based on the lattice. However, if, e.g., merging of configurations [25] is introduced to lower the complexity of the analysis, at least  $\tilde{\sqcup}'_{var}$  will be needed.

**Algorithm 5.3** Meeting Two Abstract Variable States

---

```

1: function MEETVAR( $\tilde{x}, \tilde{x}'$ )
2:    $\tilde{x}'' \leftarrow \perp_{var}$ 
3:   for all  $x \in \mathbf{Var}$  do
4:     for all  $T \in \mathbf{Thrd}$  do
5:        $\tilde{W} \leftarrow (\tilde{x}.x) T$ 
6:        $\tilde{W}' \leftarrow (\tilde{x}'.x) T$ 
7:        $C \leftarrow \emptyset$ 
8:       while  $\tilde{W} \neq \emptyset \wedge \tilde{W}' \neq \emptyset$  do
9:          $(\tilde{v}, \tilde{t}) \leftarrow \mathbf{EARLIESTWRITETHREAD}(\tilde{W})$ 
10:         $(\tilde{v}', \tilde{t}') \leftarrow \mathbf{EARLIESTWRITETHREAD}(\tilde{W}')$ 
11:         $\tilde{W} \leftarrow \tilde{W} \setminus (\tilde{v}, \tilde{t})$ 
12:         $\tilde{W}' \leftarrow \tilde{W}' \setminus (\tilde{v}', \tilde{t}')$ 
13:        if  $(\tilde{v}, \tilde{t}) = (\tilde{v}', \tilde{t}')$  then
14:           $C \leftarrow C \cup \{(\tilde{v}, \tilde{t})\}$ 
15:        else if  $\tilde{v} \sqcap_{val} \tilde{v}' \neq \perp_{val} \wedge \tilde{t} \sqcap_t \tilde{t}' \neq \perp_t \wedge \tilde{W} = \emptyset \wedge \tilde{W}' = \emptyset$  then
16:           $C \leftarrow C \cup \{(\tilde{v} \sqcap_{val} \tilde{v}', \tilde{t} \sqcap_t \tilde{t}')\}$ 
17:        else
18:           $\tilde{W} \leftarrow \emptyset$ 
19:           $\tilde{W}' \leftarrow \emptyset$ 
20:        end if
21:      end while
22:      if  $C = \emptyset$  then
23:         $((\tilde{x}'' . x) T) \leftarrow \{(\perp_{var}, \perp_t)\}$ 
24:      else
25:         $((\tilde{x}'' . x) T) \leftarrow C$ 
26:      end if
27:    end for
28:  end for
29:  return  $\tilde{x}''$ 
30: end function

```

---

**Algorithm 5.4** Joining Two Abstract Variable States

---

```

1: function JOINVAR( $\tilde{x}, \tilde{x}'$ )
2:    $\tilde{x}'' \leftarrow \tilde{\perp}_{var}$ 
3:   for all  $x \in \mathbf{Var}$  do
4:     for all  $T \in \mathbf{Thrd}$  do
5:        $\tilde{W} \leftarrow (\tilde{x} \ x) \ T$ 
6:        $\tilde{W}' \leftarrow (\tilde{x}' \ x) \ T$ 
7:        $C \leftarrow \emptyset$ 
8:        $M \leftarrow (\tilde{\perp}_{val}, \tilde{\perp}_t)$ 
9:       while  $\tilde{W} \neq \emptyset \vee \tilde{W}' \neq \emptyset$  do
10:         $\tilde{w} \leftarrow \mathbf{EARLIESTWRITETHREAD}(\tilde{W})$ 
11:         $\tilde{w}' \leftarrow \mathbf{EARLIESTWRITETHREAD}(\tilde{W}')$ 
12:        if  $\tilde{w} = \tilde{w}'$  then
13:           $C \leftarrow C \cup \{\tilde{w}\}$ 
14:           $\tilde{W} \leftarrow \tilde{W} \setminus \{\tilde{w}\}$ 
15:           $\tilde{W}' \leftarrow \tilde{W}' \setminus \{\tilde{w}'\}$ 
16:        else if  $\tilde{W} = \emptyset$  then
17:           $C \leftarrow C \cup \tilde{W}'$ 
18:           $\tilde{W}' \leftarrow \emptyset$ 
19:        else if  $\tilde{W}' = \emptyset$  then
20:           $C \leftarrow C \cup \tilde{W}$ 
21:           $\tilde{W} \leftarrow \emptyset$ 
22:        else
23:           $M \leftarrow (\bigsqcup_w \tilde{W}) \sqcup_w (\bigsqcup_w \tilde{W}')$ 
24:           $\tilde{W} \leftarrow \emptyset$ 
25:           $\tilde{W}' \leftarrow \emptyset$ 
26:        end if
27:      end while
28:       $((\tilde{x}'' \ x) \ T) \leftarrow C$ 
29:      if  $M \neq (\tilde{\perp}_{val}, \tilde{\perp}_t)$  then
30:         $((\tilde{x}'' \ x) \ T) \leftarrow ((\tilde{x}'' \ x) \ T) \cup \{M\}$ 
31:      end if
32:    end for
33:  end for
34:  return  $\tilde{x}''$ 
35: end function

```

---

**Algorithm 5.5** Write to Variable

---

```

1: function WRITE( $T, \tilde{x}, x, \tilde{w}$ )
2:    $(\tilde{x}', x') T' \leftarrow \begin{cases} ((\tilde{x} x) T) \cup \{\tilde{w}\} & \text{if } x' = x \wedge T' = T \\ (\tilde{x} x') T' & \text{otherwise} \end{cases}$ 
3:   return  $\tilde{x}'$ 
4: end function

```

---

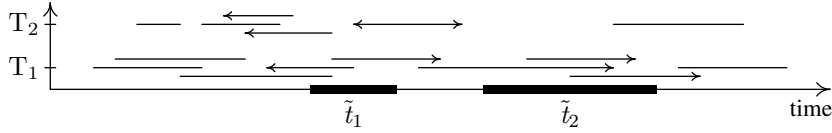


Figure 5.3: The time-stamps of the writes considered by  $\text{READ}(\tilde{x}, x, T_1, \tilde{t}_1)$  and  $\text{READ}(\tilde{x}, x, T_2, \tilde{t}_2)$ .

$\text{WRITE}(T, \tilde{x}, x, \tilde{w})$ , as defined in Algorithm 5.5, safely (Lemma 5.23) adds the write,  $\tilde{w}$ , to the set of write-history for thread  $T$ , i.e., to  $((\tilde{x} x) T)$ .

**Lemma 5.23 (Soundness of WRITE):**

Assuming that  $\tilde{x}$  contains safe write history for variable  $x$  and thread  $T$  (c.f., Definition 5.18) before the write by thread  $T$  is performed at time  $\tilde{t}$ , then so will  $\text{WRITE}(T, \tilde{x}, x, (\tilde{v}, \tilde{t}))$ .  $\square$

PROOF. Since  $\text{WRITE}(T, \tilde{x}, x, (\tilde{v}, \tilde{t}))$  simply adds the write  $(\tilde{v}, \tilde{t})$  to the history of thread  $T$ 's writes on variable  $x$  in the state  $\tilde{x}$ , and  $\tilde{x}$  is assumed to contain safe write history for  $T$  on  $x$ ,  $\text{WRITE}(T, \tilde{x}, x, (\tilde{v}, \tilde{t}))$  trivially fulfills the safety condition in Definition 5.18 with regards to  $T$  and  $x$ .  $\blacksquare$

Using the sequence and timing information provided by Definition 5.19,  $\text{READ}(\tilde{x}, x, T, \tilde{t})$ , as defined in Algorithm 5.6, only takes the writes that might be valid at  $\tilde{t}$  (the point in time when  $T$  issues the  $\text{READ}$ ) into consideration for its returned value  $\tilde{v} \in \mathbf{Val}$ , which is safe (Lemma 5.26). These writes,  $\tilde{w} = (\tilde{v}', \tilde{t}')$ , come from two categories. The first category covers the writes on  $x$  for threads  $T' \in \mathbf{Thrd} \setminus \{T\}$  whose “time-stamps” overlap in time with  $\tilde{t}$ , i.e.,  $\tilde{t} \cap \tilde{t}' \neq \perp$ . The second category covers the most recent write on  $x$  for all threads (including  $T$ ) such that its time-stamp overlaps with the overall most recent write of any write, not belonging to the first category. Note that any write for thread  $T$  with a time-stamp that begins after the beginning of  $\tilde{t}$  is discarded. So is any write for  $T' \in \mathbf{Thrd} \setminus \{T\}$  such that its time-stamp completely succeeds  $\tilde{t}$ . This is because such writes can simply not have occurred at the time of issuing the  $\text{READ}$

**Algorithm 5.6** Read from Variable

---

```

1: function READ( $\tilde{x}, x, T, \tilde{t}$ )
2:    $\tilde{x}' \leftarrow \perp_{var}$ 
3:   for all  $T' \in \text{Thrd} \setminus \{T\}$  do
4:      $((\tilde{x}' x) T') \leftarrow \{(\tilde{v}', \tilde{t}') \in ((\tilde{x} x) T') \mid \tilde{t}' \not\prec_t \tilde{t}\}$ 
5:   end for
6:    $((\tilde{x}' x) T) \leftarrow \{(\tilde{v}', \tilde{t}') \in ((\tilde{x} x) T) \mid \min(\gamma_t(\tilde{t})) \geq \min(\gamma_t(\tilde{t}'))\}$ 
7:    $\tilde{W} \leftarrow \emptyset$ 
8:   for all  $T' \in \text{Thrd} \setminus \{T\}$  do
9:      $\tilde{W}_{T'} \leftarrow \{(\tilde{v}', \tilde{t}') \in ((\tilde{x}' x) T') \mid \tilde{t}' \not\prec_t \tilde{t}\}$ 
10:     $((\tilde{x}' x) T') \leftarrow ((\tilde{x}' x) T') \setminus \tilde{W}_{T'}$ 
11:     $\tilde{W} \leftarrow \tilde{W} \cup \tilde{W}_{T'}$ 
12:   end for
13:    $\tilde{t}^{mrw} \leftarrow \text{MOSTRECENTWRITETIME}(\tilde{x}', x)$ 
14:   if  $\tilde{t}^{mrw} \neq \perp_t$  then
15:     for all  $T' \in \text{Thrd}$  do
16:        $\tilde{t}_{T'}^{mrw} \leftarrow \text{MOSTRECENTWRITETIMETHREAD}((\tilde{x}' x) T')$ 
17:        $\tilde{W} \leftarrow \tilde{W} \cup \{(\tilde{v}', \tilde{t}') \in ((\tilde{x}' x) T') \mid \tilde{t}' \not\prec_t \tilde{t}_{T'}^{mrw} \neq \perp_t \wedge \tilde{t}' \not\prec_t \tilde{t}^{mrw} \neq \perp_t\}$ 
18:     end for
19:     end if
20:      $\tilde{v} \leftarrow \begin{cases} \perp_{val} \{ \tilde{v}' \mid \exists \tilde{t}' \in \text{Time} : (\tilde{v}', \tilde{t}') \in \tilde{W} \} & \text{if } \tilde{W} \neq \emptyset \\ [-\infty, \infty] & \text{otherwise} \end{cases}$ 
21:     return  $\tilde{v}$ 
22: end function

```

---

**Algorithm 5.7** Time of Most Recent Write

---

```

1: function MOSTRECENTWRITETIME( $\tilde{x}, x$ )
2:   return MOSTRECENTWRITETIMETHREAD( $\bigcup_{T \in \text{Thrd}} ((\tilde{x} x) T)$ )
3: end function

```

---

**Algorithm 5.8** Time of Most Recent Write in Thread

---

```

1: function MOSTRECENTWRITETIMETHREAD( $\tilde{W}$ )
2:   if  $\tilde{W} = \emptyset$  then
3:     return  $\perp_t$ 
4:   end if
5:    $t_{min} \leftarrow \max(\{\min(\gamma_t(\tilde{t})) \mid \exists \tilde{v} \in \mathbf{Val} : (\tilde{v}, \tilde{t}) \in \tilde{W}\})$ 
6:    $t_{max} \leftarrow \max(\bigcup \{\gamma_t(\tilde{t}) \mid \exists \tilde{v} \in \mathbf{Val} : (\tilde{v}, \tilde{t}) \in \tilde{W} \wedge \min(\gamma_t(\tilde{t})) = t_{min}\})$ 
7:   return  $\alpha_t(\{t_{min}, t_{max}\})$ 
8: end function

```

---

(and will thus usually not be included in  $\tilde{\mathfrak{x}}$  at all). An illustration of the time-stamps of the writes in  $T_1$  and  $T_2$  that must be considered by  $\text{READ}(\tilde{\mathfrak{x}}, x, T_1, \tilde{t}_1)$  (lines with arrow heads pointing left) and  $\text{READ}(\tilde{\mathfrak{x}}, x, T_2, \tilde{t}_2)$  (lines with arrow heads pointing right) is given in Figure 5.3. The returned value,  $\tilde{v}$ , is the least upper bound of the values of the considered writes. Note that  $\text{MOSTRECENTWRITE TIME}$  and  $\text{MOSTRECENTWRITE TIME THREAD}$  are defined based on Definition 5.17 in Algorithms 5.7 and 5.8, respectively, and that these functions give the time of the most recent write among the writes in a set of writes (Lemmas 5.24 and 5.25).

**Lemma 5.24 (Soundness of  $\text{MOSTRECENTWRITE TIME THREAD}$ ):**

$\text{MOSTRECENTWRITE TIME THREAD}(\tilde{W})$ , defined in Algorithm 5.8, gives the time of the most recent write in  $\tilde{W}$ .  $\square$

PROOF. This proof will be conducted based on the structure of Algorithm 5.8.

If  $\tilde{W} = \emptyset$ , then  $\perp_t$  is returned. Otherwise,  $t_{min}$  is the greatest lower limit of the time-stamp of any write in  $\tilde{W}$  ( $\max(\{\min(\gamma_t(\tilde{t}) \mid \exists \tilde{v} \in \mathbf{Val} : (\tilde{v}, \tilde{t}) \in \tilde{W}\})$ ) and  $t_{max}$  is the greatest upper limit of the time-stamps of the writes in  $\tilde{W}$  such that the lower limit of their time-stamps are equal to  $t_{min}$  ( $\max(\bigcup\{\gamma_t(\tilde{t}) \mid \exists \tilde{v} \in \mathbf{Val} : (\tilde{v}, \tilde{t}) \in \tilde{W} \wedge \min(\gamma_t(\tilde{t})) = t_{min}\})$ ). Thus,  $\alpha(\{t_{min}, t_{max}\})$  is the time of the most recent write in  $\tilde{W}$ , as given by Definition 5.17.  $\blacksquare$

**Lemma 5.25 (Soundness of  $\text{MOSTRECENTWRITE TIME}$ ):**

$\text{MOSTRECENTWRITE TIME}(\tilde{\mathfrak{x}}, x)$ , defined in Algorithm 5.7, gives the time of the globally most recent write on  $x$  in  $\tilde{\mathfrak{x}}$ .  $\square$

PROOF. This proof is trivial since  $\text{MOSTRECENTWRITE TIME THREAD}(\tilde{W})$  is the time of the most recent write in  $\tilde{W}$  (Lemma 5.24) and the set of writes,  $\tilde{W}$ , is  $\bigcup_{T \in \mathbf{Thrd}}((\tilde{\mathfrak{x}} x) T)$ ; i.e.,  $\tilde{W}$  is a set containing the writes by all threads in  $\mathbf{Thrd}$  on  $x$ . Thus the time of the globally most recent write, as given by Definition 5.17, is returned.  $\blacksquare$

**Lemma 5.26 (Soundness of  $\text{READ}$ ):**

Assuming that  $\tilde{\mathfrak{x}}$  contains safe write history at  $\tilde{t}$  (Definition 5.18), a safe value for  $x$  at  $\tilde{t}$  as seen by thread  $T$  (Definition 5.19) is given by  $\text{READ}(\tilde{\mathfrak{x}}, x, T, \tilde{t})$ .  $\square$

PROOF. The proof amounts to showing that  $\text{READ}(\tilde{\mathfrak{x}}, x, T, \tilde{t})$  is an upper bound to the values of the writes given by Definition 5.19; i.e., to show that all writes given by Definition 5.19 are included in  $\tilde{W}$ .

On line 4, the new variable state,  $\tilde{\mathfrak{x}}'$ , is defined to contain all writes,  $(\tilde{v}', \tilde{t}') \in ((\tilde{\mathfrak{x}} x) T)$ , such that  $\tilde{t} \not\prec_t \tilde{t}'$ , for each  $T' \in \mathbf{Thrd} \setminus \{T\}$ . On lines 9–11, the writes,



$(\tilde{v}', \tilde{t}') \in ((\tilde{\mathfrak{x}}' x) T')$ , for all  $T' \in \mathbf{Thrd} \setminus \{T\}$ , such that  $\tilde{t}' \not\prec_t \tilde{t}$ , are extracted (i.e., identified and removed) from  $((\tilde{\mathfrak{x}}' x) T')$  and put in the set  $\tilde{W}$ . Thus,  $\tilde{W}$  contains all the writes specified by 1 in Definition 5.19.

On line 6,  $((\tilde{\mathfrak{x}}' x) T)$  is defined to contain all writes,  $(\tilde{v}', \tilde{t}') \in ((\tilde{\mathfrak{x}} x) T)$ , such that  $\min(\gamma_t(\tilde{t})) \geq \min(\gamma_t(\tilde{t}'))$ , and  $((\tilde{\mathfrak{x}}' x) T')$ , for each  $T' \in \mathbf{Thrd} \setminus \{T\}$ , now contains all the writes,  $(\tilde{v}', \tilde{t}') \in ((\tilde{\mathfrak{x}} x) T')$ , such that  $\tilde{t}' \prec_t \tilde{t}$ .

On line 13, the time of the (global) most recent write on  $x$  among all threads, i.e., the most recent write in  $\bigcup\{(\tilde{\mathfrak{x}}' x) T' \mid T' \in \mathbf{Thrd}\}$ , is determined (Lemma 5.25), while at line 16, the time of the most recent write for each thread is determined (Lemma 5.24). If the time of the most recent write for a thread overlaps with the time of the global most recent write, then all writes overlapping in time with the most recent write for that thread are added to  $\tilde{W}$  (line 17). Thus,  $\tilde{W}$  now also contains (at least) all the writes specified by 2 in Definition 5.19.

Finally, on line 20, the least upper bound of the values of the writes in  $\tilde{W}$  is determined. On the next line, it is returned if  $\tilde{W} \neq \emptyset$ . If  $\tilde{W} = \emptyset$ , then  $[-\infty, \infty]$  is returned, which trivially is a safe approximation of the corresponding value read (i.e.,  $v \in \gamma_{int}([-\infty, \infty])$ ) in the concrete case (c.f., Table 4.2). ■

Since  $\text{READ}(\tilde{\mathfrak{x}}, x, T, \tilde{t})$  discards writes from thread  $T' \in \mathbf{Thrd}$  that are too old to be valid at time  $\tilde{t}$  (and writes occurring after  $\tilde{t}$ ) for its returned value, and since time is assumed to never progress negatively (i.e., backwards; c.f., Lemma 4.2), the discarded writes can safely be removed from  $((\tilde{\mathfrak{x}} x) T')$ .  $\text{TRIM}$ , defined in Algorithm 5.9, safely (Lemma 5.27) removes the outdated writes from  $((\tilde{\mathfrak{x}} x) T')$  for all  $T' \in \mathbf{Thrd}$ . Thus,  $\text{TRIM}$  can be used to lower the space complexity of the analysis. Note that  $\text{SPLITSET}(\tilde{W}, \tilde{t})$ , as defined in Algorithm 5.10, is used to split a set of writes into two sets where the first set contains all writes,  $(\tilde{v}, \tilde{t}')$ , such that  $\tilde{t}' \sqcap_t \tilde{t} \neq \perp_t$ , and the second set contains all other writes.

**Lemma 5.27 (Soundness of TRIM):**

*If  $\tilde{\mathfrak{x}}$  contains safe write history at time  $\tilde{t}$  (c.f., Definition 5.18), then so does  $\text{TRIM}(\tilde{\mathfrak{x}}, \tilde{t})$ .* □

**PROOF.** Given that  $\tilde{\mathfrak{x}}$  is safe, it must be shown that, for any variable,  $x \in \mathbf{Var}$ , and any thread,  $T \in \mathbf{Thrd}$ ,  $((\text{TRIM}(\tilde{\mathfrak{x}}, \tilde{t}) x) T)$  contains at least (c.f., Definition 5.18)

1. all writes,  $(\tilde{v}, \tilde{t}')$ , of  $((\tilde{\mathfrak{x}} x) T)$  such that  $\tilde{t}' \not\prec_t \tilde{t} \wedge \tilde{t} \not\prec_t \tilde{t}'$ , and

**Algorithm 5.9** Trim Variable State

---

```

1: function TRIM( $\tilde{x}, \tilde{t}$ )
2:    $\tilde{x}' \leftarrow \tilde{\downarrow}_{var}$ 
3:    $\tilde{x}'' \leftarrow \tilde{\downarrow}_{var}$ 
4:   for all  $x \in \mathbf{Var}$  do
5:      $\langle [F_T]_{T \in \mathbf{Thrd}} \rangle \leftarrow \langle [\emptyset]_{T \in \mathbf{Thrd}} \rangle$ 
6:      $\langle [O_T]_{T \in \mathbf{Thrd}} \rangle \leftarrow \langle [\emptyset]_{T \in \mathbf{Thrd}} \rangle$ 
7:      $\langle [N_T]_{T \in \mathbf{Thrd}} \rangle \leftarrow \langle [\emptyset]_{T \in \mathbf{Thrd}} \rangle$ 
8:     for all  $T \in \mathbf{Thrd}$  do
9:        $F_T \leftarrow \{(\tilde{v}, \tilde{t}') \in (\tilde{x} \ x) \ T \mid \tilde{t} \prec_t \tilde{t}'\}$ 
10:       $(O_T, N_T) \leftarrow \mathbf{SPLITSET}((\tilde{x} \ x) \ T, \tilde{t})$ 
11:       $((\tilde{x}' \ x) \ T) \leftarrow N_T \setminus F_T$ 
12:    end for
13:     $\tilde{t}^{mrw} \leftarrow \mathbf{MOSTRECENTWRITETIME}(\tilde{x}', x)$ 
14:    for all  $T \in \mathbf{Thrd}$  do
15:       $\tilde{W}_T \leftarrow \emptyset$ 
16:       $\tilde{t}_T^{mrw} \leftarrow \mathbf{MOSTRECENTWRITETHREAD}((\tilde{x}' \ x) \ T)$ 
17:      if  $\tilde{t}_T^{mrw} \tilde{r}_t \tilde{t}^{mrw} = \tilde{\downarrow}_t \wedge F_T = \emptyset \wedge O_T = \emptyset$  then
18:         $\tilde{W}_T \leftarrow \{(\tilde{\downarrow}_{val}, \tilde{\downarrow}_t)\}$ 
19:      else
20:         $\tilde{W}_T \leftarrow \{(\tilde{v}, \tilde{t}') \in ((\tilde{x}' \ x) \ T) \mid \tilde{t}' \tilde{r}_t \tilde{t}_T^{mrw} \neq \tilde{\downarrow}_t \wedge \tilde{t}^{mrw} \tilde{r}_t \tilde{t}_T^{mrw} \neq \tilde{\downarrow}_t\}$ 
21:      end if
22:       $((\tilde{x}'' \ x) \ T) \leftarrow F_T \cup O_T \cup \tilde{W}_T$ 
23:    end for
24:  end for
25:  return  $\tilde{x}''$ 
26: end function

```

---

**Algorithm 5.10** Split Set of Writes

---

```

1: function SPLITSET( $\tilde{W}, \tilde{t}$ )
2:    $O \leftarrow \{(\tilde{v}, \tilde{t}') \in \tilde{W} \mid \tilde{t} \prec_t \tilde{t}' \wedge \tilde{t}' \not\prec_t \tilde{t}\}$ 
3:    $N \leftarrow \{(\tilde{v}, \tilde{t}') \in \tilde{W} \mid \tilde{t} \prec_t \tilde{t}' \vee \tilde{t}' \prec_t \tilde{t}\}$ 
4:   return  $(O, N)$ 
5: end function

```

---

2. any write,  $(\tilde{v}, \tilde{t}')$ , of  $((\tilde{\mathfrak{x}} x) T)$  such that  $\tilde{t}' \prec_t \tilde{t}$ , if  $\tilde{t}' \cap_t \tilde{t}^{mrw} \neq \tilde{\perp}_t$ , where  $\tilde{t}^{mrw}$  is the time of the globally most recent write of the writes preceding  $\tilde{t}$ ,

or,

3.  $(\tilde{\perp}_{val}, \tilde{\perp}_t)$ , if there are no writes fitting the definition of the previous two categories (e.g., if all writes made by  $T$  are outdated or no writes have occurred by  $T$  on  $x$ ; i.e., if  $((\tilde{\mathfrak{x}} x) T) = \{(\tilde{\perp}_{val}, \tilde{\perp}_t)\}$ ).

Before advancing to the proof procedure, note that  $\neg(\tilde{t}' \prec_t \tilde{t} \wedge \tilde{t} \prec_t \tilde{t}')$  whenever  $\tilde{t}$  or  $\tilde{t}'$  is  $\tilde{\perp}_t$  or  $\tilde{\perp}_t$ . If they are not, note that (it is implicitly assumed that **Time = Intv**):

$$\begin{aligned}
 \tilde{t}' \prec_t \tilde{t} \wedge \tilde{t} \prec_t \tilde{t}' &\stackrel{Def. 5,13}{\iff} \max(\gamma_t(\tilde{t}')) \not\prec \min(\gamma_t(\tilde{t})) \wedge \max(\gamma_t(\tilde{t})) \not\prec \min(\gamma_t(\tilde{t}')) \\
 &\stackrel{calc.}{\iff} \max(\gamma_t(\tilde{t}')) \geq \min(\gamma_t(\tilde{t})) \wedge \max(\gamma_t(\tilde{t})) \geq \min(\gamma_t(\tilde{t}')) \\
 &\stackrel{calc.}{\iff} \min(\{\max(\gamma_t(\tilde{t})), \max(\gamma_t(\tilde{t}'))\}) \geq \\
 &\qquad\qquad\qquad \max(\{\min(\gamma_t(\tilde{t})), \min(\gamma_t(\tilde{t}'))\}) \\
 &\stackrel{Def. 3,34}{\iff} \tilde{t} \cap_t \tilde{t}' \neq \tilde{\perp}_t
 \end{aligned}$$

Now, assume that  $\tilde{\mathfrak{x}}$  contains safe write history. The structure of the algorithm gives that for each  $x \in \mathbf{Var}$ :

- For each thread,  $T \in \mathbf{Thrd}$ , the set  $F_T$  contains the writes,  $(\tilde{v}, \tilde{t}')$ , by  $T$  on  $x$  such that  $\tilde{t} \prec_t \tilde{t}'$ ; i.e., writes that occur after  $\tilde{t}$ . Note that this captures all writes,  $(\tilde{v}, \tilde{t}')$ , such that  $\tilde{t}' = \tilde{\perp}_t$  as long as  $\tilde{t} \neq \tilde{\perp}_t$ .
- For each thread,  $T \in \mathbf{Thrd}$ , the set  $O_T$  contains the writes,  $(\tilde{v}, \tilde{t}')$ , by  $T$  on  $x$  such that  $\tilde{t}' \prec_t \tilde{t} \wedge \tilde{t} \prec_t \tilde{t}'$ .
- For each thread,  $T \in \mathbf{Thrd}$ , the set  $N_T$  contains the writes,  $(\tilde{v}, \tilde{t}')$ , by  $T$  on  $x$  such that  $\tilde{t}' \prec_t \tilde{t} \vee \tilde{t} \prec_t \tilde{t}'$ . Note that this captures all writes,  $(\tilde{v}, \tilde{t}')$ , such that  $\tilde{t}' = \tilde{\perp}_t$  or  $\tilde{t}' = \tilde{\perp}_t$ .
- $\tilde{t}^{mrw}$  is determined from  $\tilde{\mathfrak{x}}'$ , for which all writes,  $(\tilde{v}, \tilde{t}') \in ((\tilde{\mathfrak{x}}' x) T)$ , on  $x$  by each thread,  $T \in \mathbf{Thrd}$ , are such that  $\tilde{t}' \prec_t \tilde{t}$ .
- For each thread  $T \in \mathbf{Thrd}$ ,  $\tilde{W}_T = \{(\tilde{\perp}_{val}, \tilde{\perp}_t)\}$  whenever  $\tilde{t}_T^{mrw} \cap_t \tilde{t}^{mrw} = \tilde{\perp}_t \wedge F_T = \emptyset \wedge O_T = \emptyset$ , otherwise,  $\tilde{W}_T$  contains all the writes by  $T$  on  $x$  such that  $\tilde{t}' \prec_t \tilde{t} \wedge \tilde{t}' \cap_t \tilde{t}_T^{mrw} \neq \emptyset$  if  $\tilde{t}^{mrw} \cap_t \tilde{t}_T^{mrw} \neq \tilde{\perp}_t$ , where  $\tilde{t}_T^{mrw}$  is the time of the most recent write of the writes,  $(\tilde{v}, \tilde{t}') \in ((\tilde{\mathfrak{x}}' x) T)$ ; i.e., the writes,  $(\tilde{v}, \tilde{t}') \in ((\tilde{\mathfrak{x}} x) T)$ , such that  $\tilde{t}' \prec_t \tilde{t}$ .

Assume that  $\tilde{t}_T^{mrw} \bar{\cap}_t \tilde{t}^{mrw} \neq \perp_t \vee F_T \neq \emptyset \vee O_T \neq \emptyset$ , then  $((\tilde{x}'' x) T)$  contains all writes,  $(\tilde{v}, \tilde{t}')$ , such that  $\tilde{t} \prec_t \tilde{t}' \vee (\tilde{t}' \prec_t \tilde{t} \wedge \tilde{t} \prec_t \tilde{t}') \vee (\tilde{t}' \bar{\cap}_t \tilde{t}_T^{mrw} \neq \perp_t \wedge \tilde{t}^{mrw} \bar{\cap}_t \tilde{t}_T^{mrw} \neq \perp_t)$ . Thus conditions 1 and 2 above are fulfilled. Note that all writes,  $(\tilde{v}, \tilde{t}')$ , occurring after  $\tilde{t}$  (i.e.,  $\tilde{t} \prec_t \tilde{t}'$ ) are present in  $\tilde{x}''$ ; i.e., they are not trimmed away from  $\tilde{x}$ .

Next, assume that  $\tilde{t}_T^{mrw} \bar{\cap}_t \tilde{t}^{mrw} = \perp_t \wedge F_T = \emptyset \wedge O_T = \emptyset$ , then  $((\tilde{x}'' x) T) = \{(\tilde{\perp}_{val}, \tilde{\perp}_t)\}$ . Thus condition 3 above is fulfilled.

Thus,  $\tilde{x}''$  (and hence  $\text{TRIM}(\tilde{x}, \tilde{t})$ ) contains safe write history for all variables,  $x \in \mathbf{Var}$  and threads,  $T \in \mathbf{Thrd}$ . ■

## 5.6 Abstract Lock States

In this section, a Galois connection,  $\langle \alpha_{lock}, \gamma_{lock} \rangle$ , between the concrete domain  $\mathcal{P}(\mathbf{Lck} \rightarrow (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time}))$  and the abstract domain  $(\mathbf{Lck} \rightarrow (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time})) \cup \{\tilde{\perp}_{lock}, \tilde{\top}_{lock}\}$ , for lock states, will be defined (Theorem 5.34). The definitions of  $\gamma_{lock}$  (which is monotone by Lemma 5.33) and  $\alpha_{lock}$  are presented in Definitions 5.28 and 5.29, respectively. Note that  $\text{STT}$ ,  $\text{OWN}$ ,  $\text{DL}$ ,  $\text{POWN}$  and  $\text{REL}$  are defined in Table 5.4, and that  $\text{STT}$ ,  $\text{OWN}$ ,  $\text{DL}$ ,  $\text{POWN}$  and  $\text{REL}$  were defined in Table 4.5 on page 45.

$\tilde{\perp}$  is the bottom element,  $\tilde{\perp}_{lock}$ , if  $\exists lck \in \mathbf{Lck} : (\tilde{\perp} lck = (u, T, \tilde{\perp}_t, T', \tilde{t}) \vee \tilde{\perp} lck = (u, T, \tilde{t}, T', \tilde{\perp}_t))$  for some lock state,  $u \in \{\text{unlocked}, \text{locked}\}$ , owner,  $T \in \mathbf{Thrd}$ , and previous owner,  $T' \in \mathbf{Thrd}$ . The top element,  $\tilde{\top}_{lock}$ , identifies the mappings,  $\tilde{\top}$ , such that  $\forall lck \in \mathbf{Lck} : \tilde{\top} lck = (u, T, \tilde{\top}_t, T', \tilde{\top}_t)$ , for any lock state,  $u \in \{\text{unlocked}, \text{locked}\}$ , owner,  $T \in \mathbf{Thrd}$ , and previous owner,  $T' \in \mathbf{Thrd}$ .

**Definition 5.28 (Concretization of an abstract lock state):**

$$\left\{ \begin{array}{l} \gamma_{lock}(\tilde{\top}_{lock}) = \mathbf{Lck} \rightarrow (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time}) \\ \gamma_{lock}(\tilde{\perp}_{lock}) = \emptyset \\ \gamma_{lock}(\tilde{\top}) = \gamma_{lock}(\lambda lck \in \mathbf{Lck}. (u_{lck}, T_{lck}, \tilde{t}_{lck}, T'_{lck}, \tilde{t}'_{lck})) \\ \quad = \{ \lambda lck \in \mathbf{Lck}. (u_{lck}, T_{lck}, t_{lck}, T'_{lck}, t'_{lck}) \mid \\ \quad \quad \quad t_{lck} \in \gamma_t(\tilde{t}_{lck}) \wedge t'_{lck} \in \gamma_t(\tilde{t}'_{lck}) \} \end{array} \right. \quad \square$$

**Definition 5.29 (Abstraction of a set of lock states):**

$$\alpha_{lock}(\mathbb{L}) = \tilde{\perp}_{lock} \{ \tilde{\top} \mid \mathbb{L} \subseteq \gamma_{lock}(\tilde{\top}) \} \quad \square$$

$\begin{aligned} \mathbf{S\tilde{T}T} &: (\mathbf{Lck}_{\mathbf{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e}) \rightarrow \mathbf{Lck}_{\mathbf{stt}} \\ \mathbf{S\tilde{T}T}((u, T, \tilde{i}, T', \tilde{i}')) &= u \end{aligned}$
$\begin{aligned} \mathbf{O\tilde{W}N} &: (\mathbf{Lck}_{\mathbf{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e}) \rightarrow \mathbf{Thrd}_{\perp} \\ \mathbf{O\tilde{W}N}((u, T, \tilde{i}, T', \tilde{i}')) &= T \end{aligned}$
$\begin{aligned} \mathbf{D\tilde{L}} &: (\mathbf{Lck}_{\mathbf{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e}) \rightarrow \mathbf{Ti\tilde{m}e} \\ \mathbf{D\tilde{L}}((u, T, \tilde{i}, T', \tilde{i}')) &= \tilde{i} \end{aligned}$
$\begin{aligned} \mathbf{PO\tilde{W}N} &: (\mathbf{Lck}_{\mathbf{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e}) \rightarrow \mathbf{Thrd}_{\perp} \\ \mathbf{PO\tilde{W}N}((u, T, \tilde{i}, T', \tilde{i}')) &= T' \end{aligned}$
$\begin{aligned} \mathbf{R\tilde{E}L} &: (\mathbf{Lck}_{\mathbf{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{m}e}) \rightarrow \mathbf{Ti\tilde{m}e} \\ \mathbf{R\tilde{E}L}((u, T, \tilde{i}, T', \tilde{i}')) &= \tilde{i}' \end{aligned}$

Table 5.4: Definition of  $\mathbf{S\tilde{T}T}$ ,  $\mathbf{O\tilde{W}N}$ ,  $\mathbf{D\tilde{L}}$ ,  $\mathbf{PO\tilde{W}N}$  and  $\mathbf{R\tilde{E}L}$  – abstract versions of  $\mathbf{STT}$ ,  $\mathbf{OWN}$ ,  $\mathbf{DL}$ ,  $\mathbf{POWN}$  and  $\mathbf{REL}$ .

The partial order,  $\tilde{\sqsubseteq}_{lock}$ , greatest lower bound,  $\tilde{\sqcap}_{lock}$ , and least upper bound,  $\tilde{\sqcup}_{lock}$ , for abstract lock states follow naturally from Definitions 3.26, 3.27 and 3.28 and are presented in Definitions 5.30, 5.31 and 5.32, respectively.

**Definition 5.30 (Partial order of abstract lock states):**

$$\left\{ \begin{array}{l} \tilde{\mathbb{I}} \tilde{\sqsubseteq}_{lock} \tilde{\mathbb{I}}' \\ \tilde{\mathbb{I}} \tilde{\sqcap}_{lock} \tilde{\mathbb{I}}' \\ \tilde{\mathbb{I}} \tilde{\sqsubseteq}_{lock} \tilde{\mathbb{I}}' \iff \forall lck \in \mathbf{Lck} : (\text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{I}} lck) = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{I}}' lck) \wedge \\ \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}} lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}}' lck) \wedge \\ \text{D}\tilde{\text{L}}(\tilde{\mathbb{I}} lck) \tilde{\sqsubseteq}_t \text{D}\tilde{\text{L}}(\tilde{\mathbb{I}}' lck) \wedge \\ \text{P}\tilde{\text{O}}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}} lck) = \text{P}\tilde{\text{O}}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}}' lck) \wedge \\ \text{R}\tilde{\text{E}}\text{L}(\tilde{\mathbb{I}} lck) \tilde{\sqsubseteq}_t \text{R}\tilde{\text{E}}\text{L}(\tilde{\mathbb{I}}' lck)) \end{array} \right. \quad \square$$

**Definition 5.31 (Greatest lower bound of abstract lock states):**

$$\left\{ \begin{array}{l} \tilde{\mathbb{I}} \tilde{\sqcap}_{lock} \tilde{\mathbb{I}}' = \tilde{\mathbb{I}} \\ \tilde{\mathbb{I}} \tilde{\sqcap}_{lock} \tilde{\mathbb{I}}' = \tilde{\mathbb{I}} \\ \lambda lck \in \mathbf{Lck}. (u_1^{lck}, T_1^{lck}, \tilde{t}_1^{lck}, T_1'^{lck}, \tilde{t}_1'^{lck}) \tilde{\sqcap}_{lock} \\ \lambda lck \in \mathbf{Lck}. (u_2^{lck}, T_2^{lck}, \tilde{t}_2^{lck}, T_2'^{lck}, \tilde{t}_2'^{lck}) = \\ \left\{ \begin{array}{l} \lambda lck \in \mathbf{Lck}. \quad \text{if } \forall lck \in \mathbf{Lck} : \\ (u_1^{lck}, T_1^{lck}, \tilde{t}_1^{lck} \tilde{\sqcap}_t \tilde{t}_2^{lck}, T_1'^{lck}, \tilde{t}_1'^{lck} \tilde{\sqcap}_t \tilde{t}_2'^{lck}) \quad (u_1^{lck} = u_2^{lck} \wedge \\ T_1^{lck} = T_2^{lck} \wedge \\ T_1'^{lck} = T_2'^{lck}) \\ \tilde{\sqcap}_{lock} \quad \text{otherwise} \end{array} \right. \end{array} \right. \quad \square$$

**Definition 5.32 (Least upper bound of abstract lock states):**

$$\left\{ \begin{array}{l} \tilde{\mathbb{I}} \sqcup_{lock} \tilde{\mathbb{T}}_{lock} = \tilde{\mathbb{T}}_{lock} \sqcup_{lock} \tilde{\mathbb{I}} = \tilde{\mathbb{T}}_{lock} \\ \tilde{\mathbb{I}} \sqcup_{lock} \tilde{\mathbb{I}}_{lock} = \tilde{\mathbb{I}}_{lock} \sqcup_{lock} \tilde{\mathbb{I}} = \tilde{\mathbb{I}} \\ \lambda lck \in \mathbf{Lck}. (u_1^{lck}, T_1^{lck}, \tilde{t}_1^{lck}, T_1^{lck}, \tilde{t}_1^{lck}) \sqcup_{lock} \\ \quad \lambda lck \in \mathbf{Lck}. (u_2^{lck}, T_2^{lck}, \tilde{t}_2^{lck}, T_2^{lck}, \tilde{t}_2^{lck}) = \\ \left\{ \begin{array}{ll} \lambda lck \in \mathbf{Lck}. & \mathbf{if} \forall lck \in \mathbf{Lck} : \\ (u_1^{lck}, T_1^{lck}, \tilde{t}_1^{lck} \sqcup_t \tilde{t}_2^{lck}, T_1^{lck}, \tilde{t}_1^{lck} \sqcup_t \tilde{t}_2^{lck}) & (u_1^{lck} = u_2^{lck} \wedge \\ & T_1^{lck} = T_2^{lck} \wedge \\ & T_1^{lck} = T_2^{lck}) \\ \tilde{\mathbb{T}}_{lock} & \mathbf{otherwise} \end{array} \right. \end{array} \right. \quad \square$$

**Lemma 5.33 (Monotonicity of  $\gamma_{lock}$ ):**

$\gamma_{lock}$ , as given by Definition 5.28, is monotone.  $\square$

PROOF. Assume that  $\tilde{\mathbb{I}} \sqsubseteq_{lock} \tilde{\mathbb{I}}'$ . If  $\tilde{\mathbb{I}} = \tilde{\mathbb{I}}_{lock}$  or  $\tilde{\mathbb{I}}' = \tilde{\mathbb{T}}_{lock}$ , then trivially,  $\gamma_{lock}(\tilde{\mathbb{I}}) \subseteq \gamma_{lock}(\tilde{\mathbb{I}}')$ . Otherwise, assume that  $\mathbb{I} \in \gamma_{lock}(\tilde{\mathbb{I}})$ ,  $\tilde{\mathbb{I}} lck = (u_{lck}, T_{lck}, \tilde{t}_{lck}, T_{lck}, \tilde{t}_{lck})$  and  $\tilde{\mathbb{I}}' lck = (u'_{lck}, T'_{lck}, \tilde{t}'_{lck}, T'_{lck}, \tilde{t}'_{lck})$ . Since  $\tilde{\mathbb{I}} \sqsubseteq_{lock} \tilde{\mathbb{I}}'$ , it must be that  $\forall lck \in \mathbf{Lck} : (u_{lck} = u'_{lck} \wedge T_{lck} = T'_{lck} \wedge T_{lck} = T'_{lck} \wedge \tilde{t}_{lck} \sqsubseteq_t \tilde{t}'_{lck} \wedge \tilde{t}'_{lck} \sqsubseteq_t \tilde{t}_{lck})$ . But then, since  $\mathbb{I} \in \gamma_{lock}(\tilde{\mathbb{I}})$  and  $\gamma_t$  is monotone (Theorem 3.39), it must be that  $\mathbb{I} \in \gamma_{lock}(\tilde{\mathbb{I}}')$ . This proves the lemma.  $\blacksquare$

**Theorem 5.34 (Galois connection – Lock states):**

$\langle \alpha_{lock}, \gamma_{lock} \rangle$ , where  $\gamma_{lock}$  and  $\alpha_{lock}$  are given by Definitions 5.28 and 5.29, respectively, is a Galois connection.  $\square$

PROOF. First it will be shown that  $\gamma_{lock}$  is completely multiplicative. Thus note that  $\gamma_{lock}$  is monotone (Lemma 5.33). Next observe that  $\gamma_{lock}(\tilde{\mathbb{T}}_{lock}) = \mathbf{Lck} \rightarrow (\mathbf{Lck}_{stt} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time}) = \tilde{\mathbb{T}}_{lock}$ .

Now, assume that  $\tilde{\mathbb{I}}, \tilde{\mathbb{I}}' \in \mathbf{Lck} \rightarrow (\mathbf{Lck}_{stt} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time})$  are such that  $\tilde{\mathbb{I}} \sqsubseteq_{lock} \tilde{\mathbb{I}}' \wedge \tilde{\mathbb{I}}' \sqsubseteq_{lock} \tilde{\mathbb{I}}$ . From Definition 5.30, it follows that neither of  $\tilde{\mathbb{I}}$  and  $\tilde{\mathbb{I}}'$  can be  $\tilde{\mathbb{I}}_{lock}$  or  $\tilde{\mathbb{T}}_{lock}$ . Thus, it is safe to assume that these states can be expressed as  $\tilde{\mathbb{I}} lck = (u_{lck}, T_{lck}, \tilde{t}_{lck}, T_{lck}, \tilde{t}_{lck})$  and  $\tilde{\mathbb{I}}' lck = (u'_{lck}, T'_{lck}, \tilde{t}'_{lck}, T'_{lck}, \tilde{t}'_{lck})$ .

Based on the above assumptions, it will be shown that:

$$\gamma_{lock}(\tilde{\mathbb{I}} \sqcap_{lock} \tilde{\mathbb{I}}') = \gamma_{lock}(\tilde{\mathbb{I}}) \cap \gamma_{lock}(\tilde{\mathbb{I}}')$$

First, assume that  $\exists lck \in \mathbf{Lck} : (u_{lck} \neq u'_{lck} \vee \mathbf{T}_{lck} \neq \mathbf{T}''_{lck} \vee \mathbf{T}'_{lck} \neq \mathbf{T}'''_{lck})$ . Then,  $\tilde{\mathbb{I}} \tilde{\cap}_{lock} \tilde{\mathbb{I}}' = \tilde{\perp}_{lock}$ , and thus the L.H.S. becomes  $\gamma_{lock}(\tilde{\mathbb{I}} \tilde{\cap}_{lock} \tilde{\mathbb{I}}') = \gamma_{lock}(\tilde{\perp}_{lock}) = \emptyset$ . The R.H.S. becomes  $\gamma_{lock}(\tilde{\mathbb{I}}) \cap \gamma_{lock}(\tilde{\mathbb{I}}') = \emptyset$ , because it must be that  $\forall \mathbb{I} \in \gamma_{lock}(\tilde{\mathbb{I}}) : \forall \mathbb{I}' \in \gamma_{lock}(\tilde{\mathbb{I}}') : \mathbb{I} \neq \mathbb{I}'$  since  $\exists lck \in \mathbf{Lck} : (u_{lck} \neq u'_{lck} \vee \mathbf{T}_{lck} \neq \mathbf{T}''_{lck} \vee \mathbf{T}'_{lck} \neq \mathbf{T}'''_{lck})$ . Thus, L.H.S. = R.H.S.

Next, assume that  $\forall lck \in \mathbf{Lck} : (u_{lck} = u'_{lck} \wedge \mathbf{T}_{lck} = \mathbf{T}''_{lck} \wedge \mathbf{T}'_{lck} = \mathbf{T}'''_{lck})$  and note that  $\langle \alpha_t, \gamma_t \rangle = \langle \alpha_{int}, \gamma_{int} \rangle$  is a Galois connection (Theorem 3.39). Then,  $(\tilde{\mathbb{I}} \tilde{\cap}_{lock} \tilde{\mathbb{I}}') \text{ lck} = (u_{lck}, \mathbf{T}_{lck}, \tilde{t}_{lck} \cap_t \tilde{t}''_{lck}, \mathbf{T}'_{lck}, \tilde{t}'_{lck} \cap_t \tilde{t}'''_{lck})$  and

$$\begin{aligned} \gamma_{lock}(\tilde{\mathbb{I}} \tilde{\cap}_{lock} \tilde{\mathbb{I}}') &\stackrel{\text{Def. 5.28}}{=} \{ \lambda lck \in \mathbf{Lck}. (u_{lck}, \mathbf{T}_{lck}, t_{lck}, \mathbf{T}'_{lck}, t'_{lck}) \mid \\ &\quad t_{lck} \in \gamma_t(\tilde{t}_{lck} \cap_t \tilde{t}''_{lck}) \wedge t'_{lck} \in \gamma_t(\tilde{t}'_{lck} \cap_t \tilde{t}'''_{lck}) \} \\ &\stackrel{\text{Lem. 3.14}}{=} \{ \lambda lck \in \mathbf{Lck}. (u_{lck}, \mathbf{T}_{lck}, t_{lck}, \mathbf{T}'_{lck}, t'_{lck}) \mid \\ &\quad t_{lck} \in \gamma_t(\tilde{t}_{lck}) \cap \gamma_t(\tilde{t}''_{lck}) \wedge t'_{lck} \in \gamma_t(\tilde{t}'_{lck}) \cap \gamma_t(\tilde{t}'''_{lck}) \} \\ &\stackrel{\text{calc.}}{=} \{ \lambda lck \in \mathbf{Lck}. (u_{lck}, \mathbf{T}_{lck}, t_{lck}, \mathbf{T}'_{lck}, t'_{lck}) \mid \\ &\quad t_{lck} \in \gamma_t(\tilde{t}_{lck}) \wedge t'_{lck} \in \gamma_t(\tilde{t}'_{lck}) \} \cap \\ &\quad \{ \lambda lck \in \mathbf{Lck}. (u_{lck}, \mathbf{T}_{lck}, t_{lck}, \mathbf{T}'_{lck}, t'_{lck}) \mid \\ &\quad t_{lck} \in \gamma_t(\tilde{t}''_{lck}) \wedge t'_{lck} \in \gamma_t(\tilde{t}'''_{lck}) \} \\ &\stackrel{\text{Def. 5.28}}{=} \gamma_{lock}(\tilde{\mathbb{I}}) \cap \gamma_{lock}(\tilde{\mathbb{I}}') \end{aligned}$$

Thus, it has been shown that  $\gamma_{lock}(\tilde{\mathbb{I}} \tilde{\cap}_{lock} \tilde{\mathbb{I}}') = \gamma_{lock}(\tilde{\mathbb{I}}) \cap \gamma_{lock}(\tilde{\mathbb{I}}')$ . Now, all the three conditions in Lemma 3.4 are fulfilled, which means that  $\gamma_{lock}$  is completely multiplicative. Then, by Lemma 3.15, it is obvious that an abstraction function,  $\alpha$ , such that  $\langle \alpha, \gamma_{lock} \rangle$  is a Galois connection can be defined. Using Lemma 3.14, the definition of this  $\alpha$  is the same as that of  $\alpha_{lock}$  in Definition 5.29. Thus,  $\langle \alpha_{lock}, \gamma_{lock} \rangle$  is a Galois connection. ■

## 5.7 Abstract Configurations

In this section, a Galois connection (c.f., Theorem 5.41) between the concrete and abstract domains for configurations,  $\mathcal{P}(\mathbf{Conf})$  and  $\mathbf{C\tilde{on}f}$ , respectively, will be defined.  $\mathbf{C\tilde{on}f}$  is defined as:

$$\begin{aligned} \mathbf{C\tilde{on}f} = & (\mathcal{P}_{T \in \mathbf{Thrd}_{\tilde{e}}}(\{\mathbf{T}\} \times \mathbf{Lbl}_T \times (\mathbf{Reg}_T \rightarrow \mathbf{V\tilde{al}}) \times \mathbf{Time}) \times \\ & (\mathbf{Var} \rightarrow \mathbf{Thrd} \rightarrow \mathcal{P}(\mathbf{V\tilde{al}} \times \mathbf{Time})) \times \\ & (\mathbf{Lck} \rightarrow (\mathbf{Lck}_{\text{stt}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time} \times \mathbf{Thrd}_{\perp} \times \mathbf{Time})) \cup \\ & \{ \tilde{\perp}_{conf}, \tilde{\top}_{conf} \} \end{aligned}$$

where  $\mathbf{Thrd}_{\tilde{e}} \subseteq \mathbf{Thrd}$  (the reason for this will become apparent when the analysis is presented in Chapter 6). The abstract configuration,  $\tilde{c} \in \mathbf{C\tilde{on}f}$ , will be



denoted in the same manner as concrete configurations:

$$\tilde{c} ::= \langle [\mathbf{T}, pc_{\mathbf{T}}, \tilde{\mathbf{r}}_{\mathbf{T}}, \tilde{\mathbf{t}}_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbf{x}}, \tilde{\mathbf{l}} \rangle$$

The concretization function for abstract configurations,  $\gamma_{conf} : \mathbf{C\tilde{on}f} \rightarrow \mathcal{P}(\mathbf{Conf})$ , is given by Definition 5.35.

**Definition 5.35 (Concretization of an abstract configuration):**

$$\left\{ \begin{array}{l} \gamma_{conf}(\tilde{\mathbf{T}}_{conf}) = \mathbf{Conf} \\ \gamma_{conf}(\tilde{\mathbf{I}}_{conf}) = \emptyset \\ \gamma_{conf}(\langle [\mathbf{T}, pc_{\mathbf{T}}, \tilde{\mathbf{r}}_{\mathbf{T}}, \tilde{\mathbf{t}}_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbf{x}}, \tilde{\mathbf{l}} \rangle) = \\ \quad \{ \langle [\mathbf{T}, pc_{\mathbf{T}}, \mathbf{r}_{\mathbf{T}}, \mathbf{t}_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, \mathbf{x}, \mathbf{l} \rangle \mid \\ \quad \mathbf{r}_{\mathbf{T}} \in \gamma_{reg}(\tilde{\mathbf{r}}_{\mathbf{T}}) \wedge \mathbf{t}_{\mathbf{T}}^a \in \gamma_t(\tilde{\mathbf{t}}_{\mathbf{T}}^a) \wedge \mathbf{x} \in \gamma_{var}(\tilde{\mathbf{x}}) \wedge \mathbf{l} \in \gamma_{lock}(\tilde{\mathbf{l}}) \} \quad \square \end{array} \right.$$

The partial ordering of abstract configurations,  $\tilde{\sqsubseteq}_{conf}$ , follows naturally using Definition 3.26 and is given by Definition 5.36. Note that this relation cannot be directly used within the analysis since  $\tilde{\sqsubseteq}_{var}$  cannot. A safe relation,  $\tilde{\sqsubseteq}'_{conf}$ , is obtained by replacing  $\tilde{\sqsubseteq}_{var}$  with  $\tilde{\sqsubseteq}'_{var}$  in the definition of  $\tilde{\sqsubseteq}_{conf}$ .

**Definition 5.36 (Partial ordering of two abstract configurations):**

$$\left\{ \begin{array}{l} \tilde{c} \tilde{\sqsubseteq}_{conf} \tilde{\mathbf{T}}_{conf} \\ \tilde{\mathbf{I}}_{conf} \tilde{\sqsubseteq}_{conf} \tilde{c} \\ \langle [\mathbf{T}, pc_{\mathbf{T}}, \tilde{\mathbf{r}}_{\mathbf{T}}, \tilde{\mathbf{t}}_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbf{x}}, \tilde{\mathbf{l}} \rangle \tilde{\sqsubseteq}_{conf} \\ \quad \langle [\mathbf{T}, pc'_{\mathbf{T}}, \tilde{\mathbf{r}}'_{\mathbf{T}}, \tilde{\mathbf{t}}'^a_{\mathbf{T}}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}'}} , \tilde{\mathbf{x}}', \tilde{\mathbf{l}}' \rangle \\ \quad \iff \\ \quad \tilde{\mathbf{x}} \tilde{\sqsubseteq}'_{var} \tilde{\mathbf{x}}' \wedge \tilde{\mathbf{l}} \tilde{\sqsubseteq}_{lock} \tilde{\mathbf{l}}' \wedge \mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd}_{\tilde{c}'} \wedge \\ \quad \forall \mathbf{T} \in \mathbf{Thrd}_{\tilde{c}} : (pc_{\mathbf{T}} = pc'_{\mathbf{T}} \wedge \tilde{\mathbf{r}}_{\mathbf{T}} \tilde{\sqsubseteq}_{reg} \tilde{\mathbf{r}}'_{\mathbf{T}} \wedge \tilde{\mathbf{t}}_{\mathbf{T}}^a \tilde{\sqsubseteq}_t \tilde{\mathbf{t}}'^a_{\mathbf{T}}) \end{array} \right. \quad \square$$

The function  $\gamma_{conf}$  is monotone with respect to  $\tilde{\sqsubseteq}_{conf}$  (Lemma 5.37).

**Lemma 5.37 (Monotonicity of  $\gamma_{conf}$ ):**

The function  $\gamma_{conf} : \mathbf{C\tilde{on}f} \rightarrow \mathcal{P}(\mathbf{Conf})$  is monotone with respect to  $\tilde{\sqsubseteq}_{conf}$ . I.e., if  $\tilde{c}, \tilde{c}' \in \mathbf{C\tilde{on}f}$  and  $\tilde{c} \tilde{\sqsubseteq}_{conf} \tilde{c}'$ , then  $\gamma_{conf}(\tilde{c}) \subseteq \gamma_{conf}(\tilde{c}')$ .  $\square$

**PROOF.** Assume that  $\tilde{c}, \tilde{c}' \in \mathbf{C\tilde{on}f}$  such that  $\tilde{c} \tilde{\sqsubseteq}_{conf} \tilde{c}'$ . If  $\tilde{c} = \tilde{\mathbf{I}}_{conf}$  or  $\tilde{c}' = \tilde{\mathbf{T}}_{conf}$ , the lemma holds trivially. Otherwise,  $\tilde{c}$  and  $\tilde{c}'$  can be expressed as  $\tilde{c} =$

$\langle [T, pc_T, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_\varepsilon}, \tilde{x}, \tilde{t} \rangle$  and  $\tilde{c}' = \langle [T, pc'_T, \tilde{x}'_T, \tilde{t}'_T^a]_{T \in \mathbf{Thrd}_{\varepsilon'}}, \tilde{x}', \tilde{t}' \rangle$ . Assume that  $c \in \gamma_{conf}(\tilde{c})$ . Since  $\tilde{c} \underline{\underline{c}}_{conf} \tilde{c}'$ , it must be that:

$$\begin{aligned} \mathbf{Thrd}_{\tilde{c}} &= \mathbf{Thrd}_{\tilde{c}'} \wedge \tilde{t} \underline{\underline{t}}_{lock} \tilde{t}' \wedge \tilde{x} \underline{\underline{x}}_{var} \tilde{x}' \wedge \\ \forall T \in \mathbf{Thrd}_{\tilde{c}} : & (pc_T = pc'_T \wedge \tilde{x}_T \underline{\underline{x}}_{reg} \tilde{x}'_T \wedge \tilde{t}_T^a \underline{\underline{t}}_T^a \tilde{t}'_T^a) \end{aligned}$$

The monotonicity of  $\gamma_t$ ,  $\gamma_{reg}$ ,  $\gamma_{var}$  and  $\gamma_{lock}$  (Theorems 3.39, 5.6 and 5.10, and Lemma 5.33, respectively) then implies that  $c \in \gamma_{conf}(\tilde{c}')$  as well. Thus,  $\gamma_{conf}(\tilde{c}) \subseteq \gamma_{conf}(\tilde{c}')$  and the lemma holds. ■

The greatest lower bound operator for abstract configurations,  $\tilde{\sqcap}_{conf}$ , follows naturally using Definition 3.27 and is given by Definition 5.38. Note that this operator cannot be directly used within the analysis since  $\tilde{\sqcap}_{var}$  cannot. A safe operator,  $\tilde{\sqcap}'_{conf}$ , is obtained by replacing  $\tilde{\sqcap}_{var}$  by  $\tilde{\sqcap}'_{var}$  in the definition of  $\tilde{\sqcap}_{conf}$ .

**Definition 5.38 (Greatest lower bound for two abstract configurations):**

$$\left\{ \begin{array}{l} \tilde{c} \tilde{\sqcap}_{conf} \tilde{c}' = \tilde{\sqcap}_{conf} \tilde{\sqcap}_{conf} \tilde{c} = \tilde{c} \\ \tilde{c} \tilde{\sqcap}_{conf} \tilde{c}' = \tilde{\sqcap}_{conf} \tilde{\sqcap}_{conf} \tilde{c} = \tilde{c}' \\ \langle [T, pc_T, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_\varepsilon}, \tilde{x}, \tilde{t} \rangle \tilde{\sqcap}_{conf} \\ \langle [T, pc'_T, \tilde{x}'_T, \tilde{t}'_T^a]_{T \in \mathbf{Thrd}_{\varepsilon'}}, \tilde{x}', \tilde{t}' \rangle = \\ \left\{ \begin{array}{ll} \langle [T, pc_T, \tilde{x}_T \tilde{\sqcap}_{reg} \tilde{x}'_T, & \text{if } \mathbf{Thrd}_\varepsilon = \mathbf{Thrd}_{\varepsilon'} \wedge \\ \tilde{t}_T^a \tilde{\sqcap}_t \tilde{t}'_T^a \rangle_{T \in \mathbf{Thrd}_\varepsilon}, & \forall T \in \mathbf{Thrd}_{\tilde{c}} : pc_T = pc'_T \\ \tilde{x} \tilde{\sqcap}_{var} \tilde{x}', \tilde{t} \tilde{\sqcap}_{lock} \tilde{t}' \rangle & \end{array} \right. \\ \tilde{\sqcap}_{conf} & \text{otherwise} \end{array} \right. \quad \square$$

The least upper bound operator for abstract configurations,  $\tilde{\sqcup}_{conf}$ , follows naturally using Definition 3.28 and is given by Definition 5.39. Note that this operator cannot be directly used within the analysis since  $\tilde{\sqcup}_{var}$  cannot. A safe operator,  $\tilde{\sqcup}'_{conf}$ , is obtained by replacing  $\tilde{\sqcup}_{var}$  by  $\tilde{\sqcup}'_{var}$  in the definition of  $\tilde{\sqcup}_{conf}$ .

**Definition 5.39 (Least upper bound for two abstract configurations):**

$$\left\{ \begin{array}{l} \tilde{c} \sqcup_{conf} \tilde{\top}_{conf} = \tilde{\top}_{conf} \sqcup_{conf} \tilde{c} = \tilde{\top}_{conf} \\ \tilde{c} \sqcup_{conf} \tilde{\perp}_{conf} = \tilde{\perp}_{conf} \sqcup_{conf} \tilde{c} = \tilde{c} \\ \langle [\mathbf{T}, pc_{\mathbf{T}}, \tilde{\mathbf{i}}_{\mathbf{T}}, \tilde{\mathbf{i}}_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbf{x}}, \tilde{\mathbf{l}} \rangle \sqcup_{conf} \\ \quad \langle [\mathbf{T}, pc'_{\mathbf{T}}, \tilde{\mathbf{i}}'_{\mathbf{T}}, \tilde{\mathbf{i}}'_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}'}} , \tilde{\mathbf{x}}', \tilde{\mathbf{l}}' \rangle = \\ \left\{ \begin{array}{ll} \langle [\mathbf{T}, pc_{\mathbf{T}}, \tilde{\mathbf{i}}_{\mathbf{T}} \sqcup_{reg} \tilde{\mathbf{i}}'_{\mathbf{T}}, & \text{if } \mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd}_{\tilde{c}'} \wedge \\ \tilde{\mathbf{i}}_{\mathbf{T}}^a \sqcup_t \tilde{\mathbf{i}}'_{\mathbf{T}}^a ]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, & \forall \mathbf{T} \in \mathbf{Thrd}_{\tilde{c}} : pc_{\mathbf{T}} = pc'_{\mathbf{T}} \\ \tilde{\mathbf{x}} \sqcup_{var} \tilde{\mathbf{x}}', \tilde{\mathbf{l}} \sqcup_{lock} \tilde{\mathbf{l}}' \rangle & \\ \tilde{\top}_{conf} & \text{otherwise} \end{array} \right. \quad \square \end{array} \right.$$

The abstraction function,  $\alpha_{conf} : \mathcal{P}(\mathbf{Conf}) \rightarrow \mathbf{Conf}$ , is given by Definition 5.40 and  $\langle \alpha_{conf}, \gamma_{conf} \rangle$  is a Galois connection (Theorem 5.41).

**Definition 5.40 (Abstraction of a set of configurations):**

$$\alpha_{conf}(C) = \tilde{\sqcap}_{conf} \{ \tilde{c} \mid C \subseteq \gamma_{conf}(\tilde{c}) \} \quad \square$$

**Theorem 5.41 (Galois connection – Configurations):**

$\langle \alpha_{conf}, \gamma_{conf} \rangle$ , where  $\gamma_{conf}$  and  $\alpha_{conf}$  are given by Definitions 5.35 and 5.40, respectively, is a Galois connection.  $\square$

PROOF. First it will be shown that  $\gamma_{conf}$  is completely multiplicative. Thus note that  $\gamma_{conf}$  is monotone (Lemma 5.37). Next observe that  $\gamma_{conf}(\tilde{\top}_{conf}) = \mathbf{Conf} = \top_{conf}$ .

Now, assume that  $\tilde{c}, \tilde{c}' \in \mathbf{Conf}$  are such that  $\tilde{c} \tilde{\sqcup}_{conf} \tilde{c}' \wedge \tilde{c}' \tilde{\sqcup}_{conf} \tilde{c}$ . From Definition 5.36, it follows that neither of  $\tilde{c}$  and  $\tilde{c}'$  can be  $\tilde{\perp}_{conf}$  or  $\tilde{\top}_{conf}$ . Thus, it is safe to assume that these configurations can be expressed as  $\tilde{c} = \langle [\mathbf{T}, pc_{\mathbf{T}}, \tilde{\mathbf{i}}_{\mathbf{T}}, \tilde{\mathbf{i}}_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbf{x}}, \tilde{\mathbf{l}} \rangle$  and  $\tilde{c}' = \langle [\mathbf{T}, pc'_{\mathbf{T}}, \tilde{\mathbf{i}}'_{\mathbf{T}}, \tilde{\mathbf{i}}'_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}'}} , \tilde{\mathbf{x}}', \tilde{\mathbf{l}}' \rangle$ .

Based on the above assumptions, it will be shown that:

$$\gamma_{conf}(\tilde{c} \tilde{\sqcap}_{conf} \tilde{c}') = \gamma_{conf}(\tilde{c}) \cap \gamma_{conf}(\tilde{c}')$$

First, assume that  $\mathbf{Thrd}_{\tilde{c}} \neq \mathbf{Thrd}_{\tilde{c}'} \vee \exists \mathbf{T} \in \mathbf{Thrd}_{\tilde{c}} : pc_{\mathbf{T}} \neq pc'_{\mathbf{T}}$ . Then,  $\tilde{c} \tilde{\sqcap}_{conf} \tilde{c}' = \tilde{\perp}_{conf}$ , and thus the L.H.S. becomes  $\gamma_{conf}(\tilde{c} \tilde{\sqcap}_{conf} \tilde{c}') = \gamma_{conf}(\tilde{\perp}_{conf}) = \emptyset$ . The R.H.S. becomes  $\gamma_{conf}(\tilde{c}) \cap \gamma_{conf}(\tilde{c}') = \emptyset$ , because it must be that  $\forall c \in \gamma_{conf}(\tilde{c}) : \forall c' \in \gamma_{conf}(\tilde{c}') : c \neq c'$ , since  $\mathbf{Thrd}_{\tilde{c}} \neq \mathbf{Thrd}_{\tilde{c}'} \vee \exists \mathbf{T} \in \mathbf{Thrd}_{\tilde{c}} : pc_{\mathbf{T}} \neq pc'_{\mathbf{T}}$ . Thus, L.H.S. = R.H.S.

Next, assume that  $\mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd}_{\tilde{c}'} \wedge \forall T \in \mathbf{Thrd}_{\tilde{c}} : pc_T = pc'_T$  and note that  $\langle \alpha_t, \gamma_t \rangle = \langle \alpha_{int}, \gamma_{int} \rangle$ ,  $\langle \alpha_{reg}, \gamma_{reg} \rangle$ ,  $\langle \alpha_{var}, \gamma_{var} \rangle$  and  $\langle \alpha_{lock}, \gamma_{lock} \rangle$  are Galois connections (Theorems 3.39, 5.6, 5.10 and 5.34, respectively). Then,  $\tilde{c} \sqcap_{conf} \tilde{c}' = \langle [T, pc_T, \tilde{x}_T \sqcap_{reg} \tilde{x}'_T, \tilde{t}_T^a \sqcap_t \tilde{t}'_T]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x} \sqcap_{var} \tilde{x}', \tilde{l} \sqcap_{lock} \tilde{l}' \rangle$  and

$$\begin{aligned}
\gamma_{conf}(\tilde{c} \sqcap_{conf} \tilde{c}') &\stackrel{Def. 5.35}{=} \{ \langle [T, pc_T, \mathbb{T}_T, t_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}, \mathbb{l} \rangle \mid \\
&\quad \mathbb{T}_T \in \gamma_{reg}(\tilde{x}_T \sqcap_{reg} \tilde{x}'_T) \wedge t_T^a \in \gamma_t(\tilde{t}_T^a \sqcap_t \tilde{t}'_T) \wedge \\
&\quad \mathbb{x} \in \gamma_{var}(\tilde{x} \sqcap_{var} \tilde{x}') \wedge \mathbb{l} \in \gamma_{lock}(\tilde{l} \sqcap_{lock} \tilde{l}') \} \\
&\stackrel{Lem. 3.14}{=} \{ \langle [T, pc_T, \mathbb{T}_T, t_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}, \mathbb{l} \rangle \mid \\
&\quad \mathbb{T}_T \in \gamma_{reg}(\tilde{x}_T) \cap \gamma_{reg}(\tilde{x}'_T) \wedge t_T^a \in \gamma_t(\tilde{t}_T^a) \cap \gamma_t(\tilde{t}'_T) \wedge \\
&\quad \mathbb{x} \in \gamma_{var}(\tilde{x}) \cap \gamma_{var}(\tilde{x}') \wedge \mathbb{l} \in \gamma_{lock}(\tilde{l}) \cap \gamma_{lock}(\tilde{l}') \} \\
&\stackrel{calc.}{=} \{ \langle [T, pc_T, \mathbb{T}_T, t_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}, \mathbb{l} \rangle \mid \\
&\quad \mathbb{T}_T \in \gamma_{reg}(\tilde{x}_T) \wedge t_T^a \in \gamma_t(\tilde{t}_T^a) \wedge \\
&\quad \mathbb{x} \in \gamma_{var}(\tilde{x}) \wedge \mathbb{l} \in \gamma_{lock}(\tilde{l}) \} \cap \\
&\quad \{ \langle [T, pc_T, \mathbb{T}_T, t_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}, \mathbb{l} \rangle \mid \\
&\quad \mathbb{T}_T \in \gamma_{reg}(\tilde{x}'_T) \wedge t_T^a \in \gamma_t(\tilde{t}'_T) \wedge \\
&\quad \mathbb{x} \in \gamma_{var}(\tilde{x}') \wedge \mathbb{l} \in \gamma_{lock}(\tilde{l}') \} \\
&\stackrel{Def. 5.35}{=} \gamma_{conf}(\tilde{c}) \cap \gamma_{conf}(\tilde{c}')
\end{aligned}$$

Thus, it has been shown that  $\gamma_{conf}(\tilde{c} \sqcap_{conf} \tilde{c}') = \gamma_{conf}(\tilde{c}) \cap \gamma_{conf}(\tilde{c}')$ . Now, all the three conditions in Lemma 3.4 are fulfilled, which means that  $\gamma_{conf}$  is completely multiplicative. Then, by Lemma 3.15, it is obvious that an abstraction function,  $\alpha$ , such that  $\langle \alpha, \gamma_{conf} \rangle$  is a Galois connection can be defined. Using Lemma 3.14, the definition of this  $\alpha$  is the same as that of  $\alpha_{conf}$  in Definition 5.40. Thus,  $\langle \alpha_{conf}, \gamma_{conf} \rangle$  is a Galois connection. ■

An alternative approach to derive a Galois connection here could be to use Theorems 3.16, 3.17, 3.20, 3.22, 3.24, 3.25 and 3.39, but the presented Galois connection is easier to understand.

Now, consider the abstract domains,  $\mathbf{C\ddot{o}nf}_{in}^{ax} \ni \tilde{c}_{in}^{ax}$  and  $\mathbf{C\ddot{o}nf}_{out}^{ax} \ni \tilde{c}_{out}^{ax}$ , which will be used for the abstract axiom transition rules in Table 5.5. These domains are defined as:

$$\begin{aligned}
\mathbf{C\ddot{o}nf}_{in}^{ax} &= (\mathbf{Thrd} \times \mathbf{Lbl} \times (\mathbf{Reg} \rightarrow \mathbf{V\ddot{a}l}) \times \\
&\quad (\mathbf{Var} \rightarrow \mathbf{Thrd} \rightarrow \mathcal{P}(\mathbf{V\ddot{a}l} \times \mathbf{Ti\ddot{m}e})) \times \\
&\quad (\mathbf{Lck} \rightarrow (\mathbf{Lck}_{stt} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\ddot{m}e} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\ddot{m}e})) \times \\
&\quad \mathbf{Ti\ddot{m}e}) \cup \{ \tilde{\perp}_{in}^{ax}, \tilde{\top}_{in}^{ax} \} \\
\tilde{c}_{in}^{ax} &::= \langle T, pc, \tilde{x}, \tilde{x}', \tilde{l}, \tilde{t} \rangle
\end{aligned}$$

and:

$$\begin{aligned} \mathbf{C\tilde{on}f}_{out}^{ax} &= (\mathbf{Lbl} \times (\mathbf{Reg} \rightarrow \mathbf{V\tilde{al}}) \times \\ &\quad (\mathbf{Var} \rightarrow \mathbf{Thrd} \rightarrow \mathcal{P}(\mathbf{V\tilde{al}} \times \mathbf{Ti\tilde{me}})) \times \\ &\quad (\mathbf{Lck} \rightarrow (\mathbf{Lck}_{stt} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{me}} \times \mathbf{Thrd}_{\perp} \times \mathbf{Ti\tilde{me}}))) \cup \\ &\quad \{\perp_{out}^{ax}, \tilde{\top}_{out}^{ax}\} \\ \tilde{c}_{out}^{ax} &::= \langle pc, \tilde{r}, \tilde{x}, \tilde{l} \rangle \end{aligned}$$

It is easy to see that  $\langle \alpha_{in}^{ax}, \gamma_{in}^{ax} \rangle$  and  $\langle \alpha_{out}^{ax}, \gamma_{out}^{ax} \rangle$ , where  $\alpha_{in}^{ax} : \mathcal{P}(\mathbf{C\tilde{on}f}_{in}^{ax}) \rightarrow \mathbf{C\tilde{on}f}_{in}^{ax}$ ,  $\gamma_{in}^{ax} : \mathbf{C\tilde{on}f}_{in}^{ax} \rightarrow \mathcal{P}(\mathbf{C\tilde{on}f}_{in}^{ax})$ ,  $\alpha_{out}^{ax} : \mathcal{P}(\mathbf{C\tilde{on}f}_{out}^{ax}) \rightarrow \mathbf{C\tilde{on}f}_{out}^{ax}$  and  $\gamma_{out}^{ax} : \mathbf{C\tilde{on}f}_{out}^{ax} \rightarrow \mathcal{P}(\mathbf{C\tilde{on}f}_{out}^{ax})$  are given by Definitions 5.42, 5.43, 5.44 and 5.45, respectively, are Galois connections (c.f., Theorems 5.46 and 5.47).

**Definition 5.42 (Abstraction of a set of axiom input configurations):**

$$\alpha_{in}^{ax}(C_{in}^{ax}) = \tilde{\prod}_{in}^{ax} \{ \tilde{c}_{in}^{ax} \mid C_{in}^{ax} \subseteq \gamma_{in}^{ax}(\tilde{c}_{in}^{ax}) \} \quad \square$$

**Definition 5.43 (Concretization of an abstract axiom input configuration):**

$$\gamma_{in}^{ax}(\langle \mathbf{T}, pc, \tilde{r}, \tilde{x}, \tilde{l}, \tilde{t} \rangle) = \{ \langle \mathbf{T}, pc, r, x, l, t \rangle \mid r \in \gamma_{reg}(\tilde{r}) \wedge x \in \gamma_{var}(\tilde{x}) \wedge \\ l \in \gamma_{lock}(\tilde{l}) \wedge t \in \gamma_t(\tilde{t}) \} \quad \square$$

**Definition 5.44 (Abstraction of a set of axiom output configurations):**

$$\alpha_{out}^{ax}(C_{out}^{ax}) = \tilde{\prod}_{out}^{ax} \{ \tilde{c}_{out}^{ax} \mid C_{out}^{ax} \subseteq \gamma_{out}^{ax}(\tilde{c}_{out}^{ax}) \} \quad \square$$

**Definition 5.45 (Concretization of an abstract axiom output configuration):**

$$\gamma_{out}^{ax}(\langle pc, \tilde{r}, \tilde{x}, \tilde{l} \rangle) = \{ \langle pc, r, x, l \rangle \mid r \in \gamma_{reg}(\tilde{r}) \wedge x \in \gamma_{var}(\tilde{x}) \wedge l \in \gamma_{lock}(\tilde{l}) \} \quad \square$$

**Theorem 5.46 (Galois connection – Axiom input configurations):**

$\langle \alpha_{in}^{ax}, \gamma_{in}^{ax} \rangle$ , where  $\alpha_{in}^{ax}$  and  $\gamma_{in}^{ax}$  are given by Definitions 5.42 and 5.43, respectively, is a Galois connection. □

PROOF. Similar to the proof of Theorem 5.41. ■

**Theorem 5.47 (Galois connection – Axiom output configurations):**

$\langle \alpha_{out}^{ax}, \gamma_{out}^{ax} \rangle$ , where  $\alpha_{out}^{ax}$  and  $\gamma_{out}^{ax}$  are given by Definitions 5.44 and 5.45, respectively, is a Galois connection. □

PROOF. Similar to the proof of Theorem 5.41. ■

STM( $T, pc$ )	$\langle pc', \tilde{r}', \tilde{x}', \tilde{l}' \rangle$	If
$[\text{halt}]^{pc}$	$\langle pc, \tilde{r}, \tilde{x}, \tilde{l} \rangle$	
$[\text{skip}]^{pc}$	$\langle pc + 1, \tilde{r}, \tilde{x}, \tilde{l} \rangle$	
$[r := a]^{pc}$	$\langle pc + 1, \tilde{r}[r \mapsto \mathcal{A}[a]]\tilde{r}, \tilde{x}, \tilde{l} \rangle$	
$[\text{if } b \text{ goto } l]^{pc}$	$\langle pc + 1, \tilde{\mathcal{B}}[!b]\tilde{r}, \tilde{x}, \tilde{l} \rangle$	$\tilde{\mathcal{B}}[!b]\tilde{r} \neq \perp_{reg}$
$[\text{if } b \text{ goto } l]^{pc}$	$\langle l, \tilde{\mathcal{B}}[b]\tilde{r}, \tilde{x}, \tilde{l} \rangle$	$\tilde{\mathcal{B}}[b]\tilde{r} \neq \perp_{reg}$
$[\text{store } r \text{ to } x]^{pc}$	$\langle pc + 1, \tilde{r}, \text{WRITE}(T, \tilde{x}, x, (\tilde{r} r, \tilde{r})), \tilde{l} \rangle$	
$[\text{load } r \text{ from } x]^{pc}$	$\langle pc + 1, \tilde{r}[r \mapsto \text{READ}(\tilde{x}, x, T, \tilde{r})], \tilde{x}, \tilde{l} \rangle$	
$[\text{lock } lck]^{pc}$	$\langle pc + 1, \tilde{r}, \tilde{x}, \tilde{l}[lck \mapsto (\text{locked}, T, \text{DL}(\tilde{l} lck), \text{POWN}(\tilde{l} lck), \text{REL}(\tilde{l} lck))] \rangle$	$\text{OWN}(\tilde{l} lck) = T \wedge$ $(\text{STT}(\tilde{l} lck) = \text{unlocked} \Rightarrow$ $(\tilde{r} \not\prec_t \text{REL}(\tilde{l} lck) \wedge$ $\text{DL}(\tilde{l} lck) \not\prec_t \tilde{r}))$
$[\text{lock } lck]^{pc}$	$\langle pc, \tilde{r}, \tilde{x}, \tilde{l} \rangle$	$\text{OWN}(\tilde{l} lck) \neq T \vee$ $(\text{STT}(\tilde{l} lck) = \text{unlocked} \wedge$ $(\tilde{r} \prec_t \text{REL}(\tilde{l} lck) \vee$ $\text{DL}(\tilde{l} lck) \prec_t \tilde{r}))$
$[\text{unlock } lck]^{pc}$	$\langle pc + 1, \tilde{r}, \tilde{x}, \tilde{l}[lck \mapsto (\text{unlocked}, \perp_{thr}, \text{DL}(\tilde{l} lck), T, \tilde{r})] \rangle$	$\text{OWN}(\tilde{l} lck) = T \wedge$ $\text{STT}(\tilde{l} lck) = \text{locked}$
$[\text{unlock } lck]^{pc}$	$\langle pc + 1, \tilde{r}, \tilde{x}, \tilde{l} \rangle$	$\text{OWN}(\tilde{l} lck) \neq T \vee$ $\text{STT}(\tilde{l} lck) = \text{unlocked}$

Table 5.5:  $\langle T, pc, \tilde{r}, \tilde{x}, \tilde{l}, \tilde{r} \rangle \xrightarrow{ax} \langle pc', \tilde{r}', \tilde{x}', \tilde{l}' \rangle$ , semantics of abstract axiom transitions.

## 5.8 Abstract Semantics

The abstract transition rules for axiom statements in Table 5.5 are safe approximations of the rules in Table 4.2 with respect to Definition 5.48 (Lemma 5.49).

**Definition 5.48 (Soundness of the abstract axiom transition relation):**

Assuming that  $\tilde{\mathbb{x}}$  contains safe write history (c.f., Definition 5.18), the transition relation  $\xrightarrow[\text{ax}]{\tilde{\phantom{x}}}$  is a safe approximation of  $\xrightarrow[\text{ax}]{}_{\text{prg}}$ , as used by  $\xrightarrow[\text{prg}]{}_{\text{prg}}$ , iff

$$\forall \tilde{c}_{in}^{ax} \in \mathbf{Conf}_{in}^{ax} : \forall c_{in}^{ax} \in \gamma_{in}^{ax}(\tilde{c}_{in}^{ax}) : \forall c_{out}^{ax} \in \mathbf{Conf}_{out}^{ax} : \\ (c_{in}^{ax} \xrightarrow[\text{ax}]{} c_{out}^{ax} \Rightarrow \exists \tilde{c}_{out}^{ax} \in \mathbf{Conf}_{out}^{ax} : (\tilde{c}_{in}^{ax} \xrightarrow[\text{ax}]{\tilde{\phantom{x}}} \tilde{c}_{out}^{ax} \wedge c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})))$$

where  $c_{in}^{ax}$  is generated (c.f., Table 4.3) from a valid configuration (c.f., Definition 4.4); i.e., the lock state is valid with respect to the accumulated time of the given thread.  $\square$

**Lemma 5.49 (Soundness of  $\xrightarrow[\text{ax}]{\tilde{\phantom{x}}}$ ):**

$\xrightarrow[\text{ax}]{\tilde{\phantom{x}}}$  is a safe approximation of  $\xrightarrow[\text{ax}]{}_{\text{prg}}$ , with respect to Definition 5.48.  $\square$

PROOF. This proof will be conducted by showing for each defined transition that it is safe according to Definition 5.48.

Assume that  $\tilde{c}_{in}^{ax} @ \langle T, pc, \tilde{\mathbb{r}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}}, \tilde{t} \rangle \in \mathbf{Conf}_{in}^{ax}$  and  $c_{in}^{ax} @ \langle T, pc, r, \mathbb{x}, \mathbb{l}, t \rangle \in \mathbf{Conf}_{in}^{ax}$ , such that  $c_{in}^{ax} \in \gamma_{in}^{ax}(\tilde{c}_{in}^{ax})$ , that  $\mathbb{l}$  is valid with respect to  $t$  and that  $\mathbb{x}$  contains safe write history. Now consider each defined axiom statement.

1. Assume that  $\text{STM}(T, pc) = [\text{halt}]^{pc}$ . From the concrete semantics, it must be that  $c_{in}^{ax} \xrightarrow[\text{ax}]{} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc, r, \mathbb{x}, \mathbb{l} \rangle$ . Choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow[\text{ax}]{\tilde{\phantom{x}}} \tilde{c}_{out}^{ax}$ , i.e.,  $\tilde{c}_{out}^{ax} = \langle pc, \tilde{\mathbb{r}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle$ . Thus,  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .
2. Assume that  $\text{STM}(T, pc) = [\text{skip}]^{pc}$ . From the concrete semantics, it must be that  $c_{in}^{ax} \xrightarrow[\text{ax}]{} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc + 1, r, \mathbb{x}, \mathbb{l} \rangle$ . Choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow[\text{ax}]{\tilde{\phantom{x}}} \tilde{c}_{out}^{ax}$ , i.e.,  $\tilde{c}_{out}^{ax} = \langle pc + 1, \tilde{\mathbb{r}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle$ . Thus,  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .
3. Assume that  $\text{STM}(T, pc) = [r := a]^{pc}$ . From the concrete semantics, it must be that  $c_{in}^{ax} \xrightarrow[\text{ax}]{} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc + 1, r[r \mapsto \mathcal{A}[[a]]r], \mathbb{x}, \mathbb{l} \rangle$ . Choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow[\text{ax}]{\tilde{\phantom{x}}} \tilde{c}_{out}^{ax}$ , i.e.,  $\tilde{c}_{out}^{ax} = \langle pc + 1, \tilde{\mathbb{r}}[r \mapsto \tilde{\mathcal{A}}[[a]]\tilde{\mathbb{r}}], \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle$ . Since  $\tilde{\mathcal{A}}$  is safely induced from  $\mathcal{A}$  (see Section 5.3), it must be that  $\tilde{\mathcal{A}}[[a]]\tilde{\mathbb{r}} \in \gamma_{val}(\mathcal{A}[[a]]r)$ , and hence,  $\tilde{\mathbb{r}}[r \mapsto \tilde{\mathcal{A}}[[a]]\tilde{\mathbb{r}}] \in \gamma_{reg}(\mathbb{r}[r \mapsto \mathcal{A}[[a]]r])$ . Thus,  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .

4. Assume that  $\text{STM}(T, pc) = [\text{if } b \text{ goto } l]^{pc}$ . Then two cases must be considered.
- (a) In the first case,  $\mathcal{B}[[b]]\mathfrak{r}$ . This means that  $c_{in}^{ax} \xrightarrow{ax} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle l, \mathfrak{r}, \mathfrak{x}, \mathbb{1} \rangle$ . Now, choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow{ax} \tilde{c}_{out}^{ax}$  by the corresponding branch (i.e.,  $\tilde{\mathcal{B}}_{\mathcal{R}}[[b]]\tilde{\mathfrak{r}} \neq \tilde{\perp}_{reg}$ ); i.e.,  $\tilde{c}_{out}^{ax} = \langle l, \tilde{\mathcal{B}}_{\mathcal{R}}[[b]]\tilde{\mathfrak{r}}, \tilde{\mathfrak{x}}, \tilde{\mathbb{1}} \rangle$ . Since  $\tilde{\mathcal{B}}_{\mathcal{R}}$  is safely induced from  $\mathcal{B}$  (see Section 5.4), it must be that  $\tilde{\mathcal{B}}_{\mathcal{R}}[[b]]\tilde{\mathfrak{r}} \neq \tilde{\perp}_{reg}$  and that  $\gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$  contains, at least, all cases where  $\mathcal{B}[[b]]\mathfrak{r}$ . Thus, it must be the case that  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .
- (b) In the second case,  $\neg\mathcal{B}[[b]]\mathfrak{r}$ . This means that  $c_{in}^{ax} \xrightarrow{ax} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc + 1, \mathfrak{r}, \mathfrak{x}, \mathbb{1} \rangle$ . Now, choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow{ax} \tilde{c}_{out}^{ax}$  by the corresponding branch (i.e.,  $\tilde{\mathcal{B}}_{\mathcal{R}}[!b]\tilde{\mathfrak{r}} \neq \tilde{\perp}_{reg}$ ); i.e.,  $\tilde{c}_{out}^{ax} = \langle pc + 1, \tilde{\mathcal{B}}_{\mathcal{R}}[!b]\tilde{\mathfrak{r}}, \tilde{\mathfrak{x}}, \tilde{\mathbb{1}} \rangle$ . Since  $\tilde{\mathcal{B}}_{\mathcal{R}}$  is safely induced from  $\mathcal{B}$  (see Section 5.4), it must be that  $\tilde{\mathcal{B}}_{\mathcal{R}}[!b]\tilde{\mathfrak{r}} \neq \tilde{\perp}_{reg}$  and that  $\gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$  contains, at least, all cases where  $\neg\mathcal{B}[[b]]\mathfrak{r}$ . Thus, it must be the case that  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .
5. Assume that  $\text{STM}(T, pc) = [\text{store } r \text{ to } x]^{pc}$ . From the concrete semantics, it must be that  $c_{in}^{ax} \xrightarrow{ax} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc + 1, \mathfrak{r}, \mathfrak{x}[x \mapsto (\mathfrak{x} \ x)[T \mapsto \{(\mathfrak{r} \ r, t)\}]] \rangle$ . Choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow{ax} \tilde{c}_{out}^{ax}$ , i.e.,  $\tilde{c}_{out}^{ax} = \langle pc + 1, \tilde{\mathfrak{r}}, \text{WRITE}(T, \tilde{\mathfrak{x}}, x, (\tilde{\mathfrak{r}} \ r, \tilde{t})) \rangle$ . It is easy to see that (c.f., Algorithm 5.5)  $\mathfrak{x}[x \mapsto (\mathfrak{x} \ x)[T \mapsto \{(\mathfrak{r} \ r, t)\}]] \in \gamma_{var}(\text{WRITE}(T, \tilde{\mathfrak{x}}, x, (\tilde{\mathfrak{r}} \ r, \tilde{t})))$ , thus  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .
6. Assume that  $\text{STM}(T, pc) = [\text{load } r \text{ from } x]^{pc}$ . From the concrete semantics,  $c_{in}^{ax} \xrightarrow{ax} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc + 1, \mathfrak{r}[r \mapsto v], \mathfrak{x}, \mathbb{1} \rangle$  for some  $v$  such that  $\exists t' \in \mathbf{Time} : (v, t') \in \bigcup_{T' \in \mathbf{Thrd}}((\mathfrak{x} \ x) \ T')$  if  $\bigcup_{T' \in \mathbf{Thrd}}((\mathfrak{x} \ x) \ T') \neq \emptyset$  and  $v \in \gamma_{int}([-\infty, \infty])$  otherwise. Choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow{ax} \tilde{c}_{out}^{ax}$ , i.e.,  $\tilde{c}_{out}^{ax} = \langle pc + 1, \tilde{\mathfrak{r}}[r \mapsto \text{READ}(\tilde{\mathfrak{x}}, x, T, \tilde{t})], \tilde{\mathfrak{x}}, \tilde{\mathbb{1}} \rangle$ . Since  $\tilde{\mathfrak{x}}$  is safe at time  $\tilde{t}$  and READ then returns a safe value (Lemma 5.26), it must be that  $v \in \gamma_{val}(\text{READ}(\tilde{\mathfrak{x}}, x, T, \tilde{t}))$  and thus  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .
7. Assume that  $\text{STM}(T, pc) = [\text{lock } lck]^{pc}$ . Then two cases must be considered.
- (a) In the first case,  $\text{OWN}(\mathbb{1} \ lck) = T$ . From the concrete semantics, it must be that  $c_{in}^{ax} \xrightarrow{ax} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc + 1, \mathfrak{r}, \mathfrak{x}, \mathbb{1}[lck \mapsto$



- $(locked, T, DL(\mathbb{1} lck), POWN(\mathbb{1} lck), REL(\mathbb{1} lck))$ ). Choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow{ax} \tilde{c}_{out}^{ax}$  by the corresponding branch,  $(O\tilde{W}N(\tilde{\mathbb{1}} lck) = T \wedge (S\tilde{T}T(\tilde{\mathbb{1}} lck) = unlocked \Rightarrow (\tilde{t} \not\prec_t R\tilde{E}L(\tilde{\mathbb{1}} lck) \wedge \tilde{D}\tilde{L}(\tilde{\mathbb{1}} lck) \not\prec_t \tilde{t})))$ ; i.e.,  $\tilde{c}_{out}^{ax} = \langle pc + 1, \tilde{r}, \tilde{x}, \tilde{\mathbb{1}}[lck \mapsto (locked, T, \tilde{D}\tilde{L}(\tilde{\mathbb{1}} lck), POWN(\tilde{\mathbb{1}} lck), R\tilde{E}L(\tilde{\mathbb{1}} lck))] \rangle$ . Note that if  $STT(\mathbb{1} lck) = unlocked$ , it is implied that  $t \not\prec REL(\mathbb{1} lck) \wedge DL(\mathbb{1} lck) \not\prec t$  (Lemma 4.6). Thus, it must be the case that  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .
- (b) In the second case,  $OWN(\mathbb{1} lck) \neq T$ . From the concrete semantics, it must be that  $c_{in}^{ax} \xrightarrow{ax} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc, r, x, \mathbb{1} \rangle$ . Choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow{ax} \tilde{c}_{out}^{ax}$  by the corresponding branch,  $O\tilde{W}N(\tilde{\mathbb{1}} lck) \neq T \vee (S\tilde{T}T(\tilde{\mathbb{1}} lck) = unlocked \wedge (\tilde{t} \prec_t R\tilde{E}L(\tilde{\mathbb{1}} lck) \vee \tilde{D}\tilde{L}(\tilde{\mathbb{1}} lck) \prec_t \tilde{t}))$ ; i.e.,  $\tilde{c}_{out}^{ax} = \langle pc, \tilde{r}, \tilde{x}, \tilde{\mathbb{1}} \rangle$ . Thus, it must be the case that  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .
8. Assume that  $STM(T, pc) = [unlock lck]^{pc}$ . Then two cases must be considered.
- (a) In the first case,  $OWN(\mathbb{1} lck) = T$ . From the concrete semantics, it must be that  $c_{in}^{ax} \xrightarrow{ax} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc + 1, r, x, \mathbb{1}[lck \mapsto (unlocked, \perp_{thrd}, DL(\mathbb{1} lck), T, t)] \rangle$ . Choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow{ax} \tilde{c}_{out}^{ax}$  by the corresponding branch,  $O\tilde{W}N(\tilde{\mathbb{1}} lck) = T \wedge S\tilde{T}T(\tilde{\mathbb{1}} lck) = locked$ ; i.e.,  $\tilde{c}_{out}^{ax} = \langle pc + 1, \tilde{r}, \tilde{x}, \tilde{\mathbb{1}}[lck \mapsto (unlocked, \perp_{thrd}, \tilde{D}\tilde{L}(\tilde{\mathbb{1}} lck), T, \tilde{t})] \rangle$ . Note that in the concrete case,  $STT(\mathbb{1} lck) = locked$  whenever  $OWN(\mathbb{1} lck) \neq \perp_{thrd}$  for a valid configuration (Definition 4.4). Thus, it must be the case that  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ .
- (b) In the second case,  $OWN(\mathbb{1} lck) \neq T$ . From the concrete semantics, it must be that  $c_{in}^{ax} \xrightarrow{ax} c_{out}^{ax}$ , where  $c_{out}^{ax} = \langle pc + 1, r, x, \mathbb{1} \rangle$ . Choose  $\tilde{c}_{out}^{ax}$  so that  $\tilde{c}_{in}^{ax} \xrightarrow{ax} \tilde{c}_{out}^{ax}$  by the corresponding branch,  $O\tilde{W}N(\tilde{\mathbb{1}} lck) \neq T \vee S\tilde{T}T(\tilde{\mathbb{1}} lck) = unlocked$ ; i.e.,  $\tilde{c}_{out}^{ax} = \langle pc + 1, \tilde{r}, \tilde{x}, \tilde{\mathbb{1}} \rangle$ . Thus, it must be the case that  $c_{out}^{ax} \in \gamma_{out}^{ax}(\tilde{c}_{out}^{ax})$ . ■

$$\frac{\mathbf{Thrd}_{exe} \neq \emptyset \wedge \forall T \in \mathbf{Thrd}_{exe} : \langle T, pc_T, \tilde{\mathfrak{r}}_T, \tilde{\mathfrak{x}}, \tilde{\mathfrak{l}}', \tilde{t}_T^a \rangle \xrightarrow{\tilde{\alpha}} \langle pc'_T, \tilde{\mathfrak{r}}'_T, \tilde{\mathfrak{x}}'_T, \tilde{\mathfrak{l}}' \rangle}{\tilde{c} @ \langle [T, pc_T, \tilde{\mathfrak{r}}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_e}, \tilde{\mathfrak{x}}, \tilde{\mathfrak{l}} \rangle \xrightarrow{prg} \tilde{c}' @ \langle [T, (T \in \mathbf{Thrd}_{exe} ? pc'_T : pc_T), (T \in \mathbf{Thrd}_{exe} ? \tilde{\mathfrak{r}}'_T : \tilde{\mathfrak{r}}_T), \tilde{t}_T^a]_{T \in \mathbf{Thrd}_e}, \tilde{\mathfrak{x}}', \tilde{\mathfrak{l}}' \rangle}$$

where

$$\tilde{t}_T^i = \text{ABSTIME}(\tilde{c}, T)$$

$$\tilde{t}_{all} = \alpha_t(\{\min(\{\min(\{\gamma_t(\tilde{t}_T^a \dot{-} \tilde{t}_T^i)\} | B)\}, \min(\{\max(\{\gamma_t(\tilde{t}_T^a \dot{-} \tilde{t}_T^i)\} | B)\})) \quad \text{where } B \iff T \in \mathbf{Thrd}_e \wedge \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T} \wedge \forall lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \Rightarrow \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathfrak{l}}' lck) \in \{\perp_{thrd}, T\})$$

$$\mathbf{Thrd}_{exe}^{all} = \{T \in \mathbf{Thrd}_e \mid \tilde{t}_{all} \dot{\cap}_t (\tilde{t}_T^a \dot{-} \tilde{t}_T^i) \neq \perp_t \wedge \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}\}$$

$$\tilde{\mathfrak{l}}' lck = \begin{cases} (\text{unlocked}, T', \text{DLLOCK}(\tilde{c}, lck), & \text{for some } T' \in \{T \in \mathbf{Thrd}_e \mid \exists l \in \mathbf{Lbl}_T : \text{STM}(T, l) = [\text{lock } lck]^l\}, \\ \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathfrak{l}}' lck), \text{R}\tilde{\text{E}}\text{L}(\tilde{\mathfrak{l}}' lck)) & \text{if } \exists T \in \mathbf{Thrd}_{exe}^{all} : \text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathfrak{l}}' lck) = \perp_{thrd} \\ \tilde{\mathfrak{l}}' lck & \text{otherwise} \end{cases}$$

$$\mathbf{Thrd}_{hold} = \{T \in \mathbf{Thrd}_e \mid \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathfrak{l}}' lck) \neq T) \vee \text{STM}(T, pc_T) = [\text{halt}]^{pc_T}\}$$

$$\tilde{t} = \alpha_t(\{\min(\{\min(\{\gamma_t(\tilde{t}_T^a \dot{-} \tilde{t}_T^i)\} | T \in \mathbf{Thrd}_e \setminus \mathbf{Thrd}_{hold})\}, \min(\{\max(\{\gamma_t(\tilde{t}_T^a \dot{-} \tilde{t}_T^i)\} | T \in \mathbf{Thrd}_e \setminus \mathbf{Thrd}_{hold})\}))$$

$$\mathbf{Thrd}_{exe} = \{T \in \mathbf{Thrd}_e \setminus \mathbf{Thrd}_{hold} \mid \tilde{t} \dot{\cap}_t (\tilde{t}_T^a \dot{-} \tilde{t}_T^i) \neq \perp_t\}$$

$$\tilde{\mathfrak{l}}' lck = \begin{cases} \tilde{\mathfrak{l}}'_{\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathfrak{l}}' lck)} lck & \text{if } \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathfrak{l}}' lck) \in \mathbf{Thrd}_{exe} \\ \tilde{\mathfrak{l}}' lck & \text{otherwise} \end{cases}$$

$$\tilde{\mathfrak{x}}' = \begin{cases} \text{TRIM}(\tilde{\mathfrak{x}}'', \tilde{t}) & \text{if } \mathbf{Thrd}_e = \mathbf{Thrd} \\ \tilde{\mathfrak{x}}'' & \text{otherwise} \end{cases} \quad \text{where } (\tilde{\mathfrak{x}}'' x) T = \begin{cases} (\tilde{\mathfrak{x}}'_T x) T & \text{if } T \in \mathbf{Thrd}_{exe} \\ (\tilde{\mathfrak{x}} x) T & \text{otherwise} \end{cases}$$

$$\tilde{t}_T^a = \text{ACCTIME}(\langle [T', pc_{T'}, \tilde{\mathfrak{r}}_{T'}, \tilde{t}_{T'}^a]_{T' \in \mathbf{Thrd}_e}, \tilde{\mathfrak{x}}, \tilde{\mathfrak{l}}'', \mathbf{Thrd}_{exe}, T)$$
Table 5.6:  $\tilde{c} \xrightarrow{prg} \tilde{c}'$ , semantics of abstract program transitions.

The abstract transition rule for program configurations in Table 5.6 is an approximation of the concrete rule in Table 4.3. The abstract rule now defines a window in time,  $\tilde{t}$ , (since **Time** = **Intv**) that determines which threads are included in  $\mathbf{Thrd}_{exe}$ . The window reaches from the earliest point in time when some thread might execute its active statements, to the earliest point in time when some thread must execute its active statements. Note that DLLOCK and ACCTIME are defined in Algorithms 5.11 and 5.12, respectively, and that ABSTIME is assumed to be a safe approximation of TIME, as specified in Assumption 5.50; however, the definitions of these functions are out of the scope for this thesis.

**Assumption 5.50 (ABSTIME is safe and non-negative):**

*It is assumed that ABSTIME is a “non-negative” function that safely approximates TIME in the interval domain. More formally, it is assumed that*

$$\forall \tilde{c} @ \langle [T, pc_T, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle \in \mathbf{C\ddot{o}nf} : \\ \forall T \in \mathbf{Thrd}_{\tilde{c}} : 0 \leq \min(\gamma_i(\mathbf{ABSTIME}(\tilde{c}, T)))$$

and

$$\forall \tilde{c} @ \langle [T, pc_T^{\tilde{c}}, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle \in \mathbf{C\ddot{o}nf} : \\ \forall c @ \langle [T, pc_T, r_T, t_T^a]_{T \in \mathbf{Thrd}}, x, l \rangle \in \mathbf{Conf} : \\ (\mathbf{Thrd}_{\tilde{c}} \subseteq \mathbf{Thrd} \Rightarrow \forall T \in \mathbf{Thrd}_{\tilde{c}} : ((pc_T = pc_T^{\tilde{c}} \wedge t_T^a \in \gamma_i(\tilde{t}_T^a)) \Rightarrow \\ \mathbf{TIME}(c, T) \in \gamma_i(\mathbf{ABSTIME}(\tilde{c}, T)))) \quad \square$$

**Algorithm 5.11** Determine Deadline for Lock Owner Assignment

---

```

1: function DLLOCK( $\tilde{c} @ \langle [\mathbb{T}', pc_{\mathbb{T}'}, \tilde{\mathbb{T}}_{\mathbb{T}'}, \tilde{t}_{\mathbb{T}'}^a]_{\mathbb{T}' \in \text{Thrd}_e}, \tilde{\mathbb{x}}, \tilde{\mathbb{I}} \rangle, lck$ )
2:    $\tilde{t}_{dl} \leftarrow \tilde{\tau}_t$ 
3:   for all  $\mathbb{T} \in \text{Thrd}_e$  do
4:     if  $\text{STM}(\mathbb{T}, pc_{\mathbb{T}}) = [\text{lock } lck]^{pc_{\mathbb{T}}}$  then
5:        $\tilde{c}' \leftarrow \tilde{c}$ 
6:        $\tilde{t}_{\mathbb{T}}^{a'} \leftarrow \tilde{t}_{\mathbb{T}}^a$ 
7:       repeat
8:          $\tilde{c}' \leftarrow \langle [\mathbb{T}', pc_{\mathbb{T}'}, \tilde{\mathbb{T}}_{\mathbb{T}'}, (\mathbb{T} = \mathbb{T}' ? \tilde{t}_{\mathbb{T}'}^{a'} : \tilde{t}_{\mathbb{T}'}^a)]_{\mathbb{T}' \in \text{Thrd}_e}, \tilde{\mathbb{x}}, \tilde{\mathbb{I}} \rangle$ 
9:          $\tilde{t}_{\mathbb{T}}^{a'} \leftarrow \tilde{t}_{\mathbb{T}}^{a'} \dot{+}_t \text{ABSTIME}(\tilde{c}', \mathbb{T})$ 
10:        until  $\text{REL}(\tilde{\mathbb{I}} lck) \lesssim_t \tilde{t}_{\mathbb{T}}^{a'} \vee 0 \in \gamma_t(\text{ABSTIME}(\tilde{c}', \mathbb{T}))$ 
11:        if  $\text{REL}(\tilde{\mathbb{I}} lck) \not\lesssim_t \tilde{t}_{\mathbb{T}}^{a'} \wedge 0 \in \gamma_t(\text{ABSTIME}(\tilde{c}', \mathbb{T}))$  then
12:           $\tilde{t} \leftarrow \tilde{t}_{\mathbb{T}}^{a'} \sqcup_t \text{REL}(\tilde{\mathbb{I}} lck)$ 
13:           $\tilde{c}' \leftarrow \langle [\mathbb{T}', pc_{\mathbb{T}'}, \tilde{\mathbb{T}}_{\mathbb{T}'}, (\mathbb{T} = \mathbb{T}' ? \tilde{t} : \tilde{t}_{\mathbb{T}'}^a)]_{\mathbb{T}' \in \text{Thrd}_e}, \tilde{\mathbb{x}}, \tilde{\mathbb{I}} \rangle$ 
14:           $\tilde{t}_{dl} \leftarrow \tilde{t}_{dl} \dot{\cap}_t ((\tilde{t} \dot{+}_t \text{ABSTIME}(\tilde{c}', \mathbb{T})) \sqcup_t \alpha_t(\{-\infty\}))$ 
15:        else
16:           $\tilde{t}_{dl} \leftarrow \tilde{t}_{dl} \dot{\cap}_t (\tilde{t}_{\mathbb{T}}^{a'} \sqcup_t \alpha_t(\{-\infty\}))$ 
17:        end if
18:      end if
19:    end for
20:    return  $\tilde{t}_{dl}$ 
21: end function

```

---

**Algorithm 5.12** Determine Accumulated Execution Time

---

```

1: function ACCTIME( $\tilde{c} @ \langle [\mathbb{T}', pc_{\mathbb{T}'}, \tilde{\mathbb{T}}_{\mathbb{T}'}, \tilde{t}_{\mathbb{T}'}^a]_{\mathbb{T}' \in \text{Thrd}_e}, \tilde{\mathbb{x}}, \tilde{\mathbb{I}} \rangle, \text{Thrd}_{exe}, \mathbb{T}$ )
2:    $\tilde{t}_{\mathbb{T}}^{a'} \leftarrow \tilde{t}_{\mathbb{T}}^a$ 
3:   if  $\mathbb{T} \in \text{Thrd}_{exe}$  then
4:      $\tilde{t}_{\mathbb{T}}^r \leftarrow \text{ABSTIME}(\tilde{c}, \mathbb{T})$ 
5:     if  $\forall lck \in \text{Lck} : \text{STM}(\mathbb{T}, pc_{\mathbb{T}}) \neq [\text{lock } lck]^{pc_{\mathbb{T}}}$  then
6:        $\tilde{t}_{\mathbb{T}}^{a'} \leftarrow \tilde{t}_{\mathbb{T}}^a \dot{+}_t \tilde{t}_{\mathbb{T}}^r$ 
7:     else

```

---

**Algorithm 5.12 Cont.** Determine Accumulated Execution Time

---

```

8:   for all  $lck \in \mathbf{Lck}$  do
9:     if  $\text{STM}(\mathbf{T}, pc_{\mathbf{T}}) = [\text{lock } lck]^{pc_{\mathbf{T}}} \wedge \text{OWN}(\tilde{\mathbb{I}} lck) = \mathbf{T}$  then
10:      if  $\text{STT}(\tilde{\mathbb{I}} lck) = \text{locked}$  then
11:         $\tilde{t}_{\mathbf{T}}^{a'} \leftarrow \tilde{t}_{\mathbf{T}}^a \dot{+}_t \tilde{t}_{\mathbf{T}}^r$ 
12:      else if  $\tilde{\text{DL}}(\tilde{\mathbb{I}} lck) \prec_t (\tilde{t}_{\mathbf{T}}^a \dot{+}_t \tilde{t}_{\mathbf{T}}^r)$  then
13:         $\tilde{t}_{\mathbf{T}}^{a'} \leftarrow \tilde{t}_{\mathbf{T}}^a \dot{+}_t \tilde{t}_{\mathbf{T}}^r$ 
14:      else if  $(\tilde{t}_{\mathbf{T}}^a \dot{+}_t \tilde{t}_{\mathbf{T}}^r) \prec_t \text{REL}(\tilde{\mathbb{I}} lck)$  then
15:         $\tilde{c}' \leftarrow \tilde{c}$ 
16:        while  $(\tilde{t}_{\mathbf{T}}^{a'} \dot{+}_t \text{ABSTIME}(\tilde{c}', \mathbf{T})) \prec_t \text{REL}(\tilde{\mathbb{I}} lck)$  do
17:           $\tilde{t}_{\mathbf{T}}^{a'} \leftarrow \tilde{t}_{\mathbf{T}}^{a'} \dot{+}_t \text{ABSTIME}(\tilde{c}', \mathbf{T})$ 
18:           $\tilde{c}' \leftarrow \langle [\mathbf{T}', pc_{\mathbf{T}'}, \tilde{\pi}_{\mathbf{T}'}, (\mathbf{T} = \mathbf{T}' ? \tilde{t}_{\mathbf{T}}^{a'} : \tilde{t}_{\mathbf{T}}^a)]_{\mathbf{T}' \in \text{Thrd}_e, \tilde{\mathbb{X}}, \tilde{\mathbb{I}}} \rangle$ 
19:        end while
20:      else if  $\text{POWN}(\tilde{\mathbb{I}} lck) = \mathbf{T} \vee \text{REL}(\tilde{\mathbb{I}} lck) \prec_t (\tilde{t}_{\mathbf{T}}^a \dot{+}_t \tilde{t}_{\mathbf{T}}^r)$  then
21:         $\tilde{t}_{\mathbf{T}}^{a'} \leftarrow (\tilde{t}_{\mathbf{T}}^a \dot{+}_t \tilde{t}_{\mathbf{T}}^r) \dot{\cap}_t \tilde{\text{DL}}(\tilde{\mathbb{I}} lck)$ 
22:      else
23:         $\triangleright \text{STT}(\tilde{\mathbb{I}} lck) = \text{unlocked} \wedge \text{REL}(\tilde{\mathbb{I}} lck) \dot{\cap}_t (\tilde{t}_{\mathbf{T}}^a \dot{+}_t \tilde{t}_{\mathbf{T}}^r) \neq \tilde{\perp}_t \wedge$ 
24:         $\text{POWN}(\tilde{\mathbb{I}} lck) \neq \mathbf{T} \wedge \tilde{\text{DL}}(\tilde{\mathbb{I}} lck) \not\prec_t (\tilde{t}_{\mathbf{T}}^a \dot{+}_t \tilde{t}_{\mathbf{T}}^r)$ 
25:         $\tilde{t}_{\mathbf{T}}^{a''} \leftarrow \tilde{t}_{\mathbf{T}}^a \dot{+}_t \tilde{t}_{\mathbf{T}}^r$ 
26:         $\tilde{c}' \leftarrow \tilde{c}$ 
27:        repeat
28:          if  $\tilde{\text{DL}}(\tilde{\mathbb{I}} lck) \prec_t (\tilde{t}_{\mathbf{T}}^{a''} \dot{+}_t \text{ABSTIME}(\tilde{c}', \mathbf{T}))$  then
29:             $\tilde{t}_{\mathbf{T}}^{a''} \leftarrow \tilde{t}_{\mathbf{T}}^{a''} \dot{+}_t \text{ABSTIME}(\tilde{c}', \mathbf{T})$ 
30:          else if  $0 \in \gamma_t(\text{ABSTIME}(\tilde{c}', \mathbf{T}))$  then
31:             $\tilde{t} \leftarrow (\tilde{t}_{\mathbf{T}}^{a''} \dot{\sqcup}_t \alpha_t(\{\infty\})) \dot{\cap}_t \text{REL}(\tilde{\mathbb{I}} lck)$ 
32:             $\tilde{c}' \leftarrow \langle [\mathbf{T}', pc_{\mathbf{T}'}, \tilde{\pi}_{\mathbf{T}'}, (\mathbf{T} = \mathbf{T}' ? \tilde{t} : \tilde{t}_{\mathbf{T}}^a)]_{\mathbf{T}' \in \text{Thrd}_e, \tilde{\mathbb{X}}, \tilde{\mathbb{I}}} \rangle$ 
33:             $\tilde{t}_{\mathbf{T}}^{a''} \leftarrow \tilde{t} \dot{+}_t \text{ABSTIME}(\tilde{c}', \mathbf{T})$ 
34:             $\tilde{t}_{\mathbf{T}}^{a''} \leftarrow \tilde{t}_{\mathbf{T}}^{a''} \dot{+}_t \text{ABSTIME}(\tilde{c}', \mathbf{T})$ 
35:          else if
36:             $\tilde{c}' \leftarrow \langle [\mathbf{T}', pc_{\mathbf{T}'}, \tilde{\pi}_{\mathbf{T}'}, (\mathbf{T} = \mathbf{T}' ? \tilde{t}_{\mathbf{T}}^{a''} : \tilde{t}_{\mathbf{T}}^a)]_{\mathbf{T}' \in \text{Thrd}_e, \tilde{\mathbb{X}}, \tilde{\mathbb{I}}} \rangle$ 
37:          end if
38:          until  $\tilde{t}_{\mathbf{T}}^{a''} = \tilde{t}_{\mathbf{T}}^{a''} \vee \text{REL}(\tilde{\mathbb{I}} lck) \prec_t \tilde{t}_{\mathbf{T}}^{a''}$ 
39:           $\tilde{t}_{\mathbf{T}}^{a''} \leftarrow (\tilde{t}_{\mathbf{T}}^{a''} \dot{\sqcup}_t \tilde{t}_{\mathbf{T}}^{a''}) \dot{\cap}_t \tilde{\text{DL}}(\tilde{\mathbb{I}} lck) \dot{\cap}_t (\text{REL}(\tilde{\mathbb{I}} lck) \dot{\sqcup}_t \alpha_t(\{\infty\}))$ 
40:        end if
41:      end if
42:    end for
43:  end if
44:  return  $\tilde{t}_{\mathbf{T}}^{a'}$ 
45: end function

```

---

Since **Time** is approximated using **Time**, there are some consequences, rendering  $\xrightarrow[\text{prg}]{\sim}$  an unsafe approximation of  $\xrightarrow[\text{prg}]{} (c.f., \text{Tables 4.3 and 5.6})$  in the general case.

1. The sets of threads to execute, i.e.,  $\mathbf{Thrd}_{exe}$ , might differ between  $c \in \mathbf{Conf}$  and  $\tilde{c} \in \mathbf{C\tilde{on}f}$ , even if  $c \in \gamma_{conf}(\tilde{c})$ . Because of this, different program points might be “visited” in the concrete and abstract cases, and thus, fixed-point calculations on  $\xrightarrow[\text{prg}]{\sim}$  in the traditional sense cannot be used to find a safe over-approximation of the concrete collecting semantics (see for example [14, 23]).
2. The execution of load-statements cannot be safely approximated using  $\xrightarrow[\text{prg}]{\sim}$  if  $|\mathbf{Thrd}_{exe}| > 1$  and the value of a global variable is to be loaded. The reason for this is that executing load-statements introduces data-dependencies between the threads, and the READ-function could return a value for which all possible writes have not been taken into account; i.e., all store-statements that could affect the variable have not yet been executed (and thus,  $\tilde{x}$  does not contain safe write history). To see this, assume that for some abstract configuration,  $\mathbf{Thrd}_{exe} = \{T_1, T_2\}$ ,  $\text{STM}(T_1, pc_{T_1}) = [\text{load } r \text{ from } x]^{pc_{T_1}}$ ,  $\text{STM}(T_2, pc_{T_2}) = [\text{skip}]^{pc_{T_2}}$  and  $\text{STM}(T_2, pc_{T_2} + 1) = [\text{store } r' \text{ to } x]^{pc_{T_2} + 1}$ . When a transition occurs, the load- and skip-statements are considered. However, since the execution time of the store-statement (the abstract “point” in time when the thread’s  $pc$  is updated) overlaps with the execution time of the load-statement, the resulting value of  $r$  in  $T_1$  should be affected by the value of  $r'$  in  $T_2$ , but this will not be the case.
3. A similar reasoning to that for load-statements holds for lock-statements – an unlocked lock,  $lck \in \mathbf{Lck}$ , cannot simply be assigned to one of the threads in  $\mathbf{Thrd}_{exe}$  that issues `lock lck`. This is because in the concrete case, the lock might be assigned to another thread in  $\mathbf{Thrd}_{exe}$  (that might not yet be executing `lock lck` in the abstract case). Thus, the only safe option is to make assignments to, at least, each thread specified in the considered abstract configuration that at some point might acquire  $lck$ . This is because these threads (even if currently not in  $\mathbf{Thrd}_{exe}$ ) could compete for  $lck$  with subsequent statements. If a thread that has been assigned  $lck$  actually does not compete for  $lck$ , this can be detected if the thread reaches a `halt`-statement or using the deadline parameter in the state for  $lck$ .

4. A transition sequence containing deadlocked configurations will not be safely approximated. In the concrete case, the threads included in the deadlock are spinning on the locks they are waiting to acquire. This means that time moves forward for these threads (given that TIME is non-zero). However, in the abstract case, the threads will be frozen and their accumulated times do not increase on a transition.

To handle these issues, the analysis will be proven to safely approximate the timing bounds of any concrete configuration,  $c@ \langle [T, pc_T, \mathbb{T}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{I} \rangle \in \mathbf{Conf}$ , in the finite collecting semantics,  $\mathcal{C}(C)$ , of a program in the initial states described by the configurations in  $C$ , such that  $\forall T \in \mathbf{Thrd} : \text{STM}(T, pc_T) = [\text{halt}]^{pc_T}$ . The analysis will also be proven to safely approximate the timing bounds of some (but not all) collecting semantics that might be infinite. More on this in Chapter 6.

$\xrightarrow[\text{prg}]{\sim}$  will be proven to be a safe approximation of  $\xrightarrow[\text{prg}]{}$  in any finite collecting semantics, with respect to each thread individually, for any configuration,  $\tilde{c}@ \langle [T, pc_T, \mathbb{T}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_e}, \tilde{\mathbb{x}}, \tilde{\mathbb{I}} \rangle \in \mathbf{Conf}$ , such that  $|\mathbf{Thrd}_{exe}| \neq 1 \vee \{T \in \mathbf{Thrd}_{exe} \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : \text{STM}(T, pc_T) = [\text{load } r \text{ from } x]^{pc_T}\} = \emptyset$ , where  $\mathbf{Var}_g$  is the set of all global variables (i.e., variables that might transfer data between threads); i.e., either no thread issues a load-statement on a global variable, or there is such a thread and it is the sole thread that is executed, which means that  $\tilde{\mathbb{x}}$  must contain safe write history since no more writes on  $x$  can occur before the given load-statement has been executed.

One thing to notice from how  $\xrightarrow[\text{prg}]{\sim}$  is defined is that an abstract configuration cannot have the same restrictions for it being valid as a concrete configuration does (c.f., Definition 4.4). When a thread (in  $\mathbf{Thrd}_{exe}$ ) wants to acquire some unlocked lock,  $\xrightarrow[\text{prg}]{\sim}$  can assign the lock to any thread that at some point in the program wants to acquire the lock, as discussed in 3 above. However (quite obviously), the assigned thread might not acquire the lock with its current statement (it is also possible that the thread never acquires the lock at all with its future statements). Therefore, an abstract configuration,  $\tilde{c}@ \langle [T, pc_T, \mathbb{T}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_e}, \tilde{\mathbb{x}}, \tilde{\mathbb{I}} \rangle \in \mathbf{Conf}$ , must be considered temporarily valid even if  $\exists lck \in \mathbf{Lck} : (\text{O}\tilde{\mathbf{W}}\mathbf{N}(\tilde{\mathbb{I}} lck) \neq \perp_{\text{thrd}} \wedge \text{S}\tilde{\mathbf{T}}\mathbf{T}(\tilde{\mathbb{I}} lck) = \text{unlocked})$ . As also discussed in 3 above, however, such an abstract configuration can be considered invalid if  $\exists lck \in \mathbf{Lck} : (\text{O}\tilde{\mathbf{W}}\mathbf{N}(\tilde{\mathbb{I}} lck) \neq \perp_{\text{thrd}} \wedge \text{S}\tilde{\mathbf{T}}\mathbf{T}(\tilde{\mathbb{I}} lck) = \text{unlocked} \wedge (\text{D}\tilde{\mathbf{L}}(\tilde{\mathbb{I}} lck) \prec_t (\tilde{t}_{\text{O}\tilde{\mathbf{W}}\mathbf{N}(\tilde{\mathbb{I}} lck)}^a \dot{+}_t \text{ABSTIME}(\tilde{c}, \text{O}\tilde{\mathbf{W}}\mathbf{N}(\tilde{\mathbb{I}} lck))) \vee \text{STM}(\text{O}\tilde{\mathbf{W}}\mathbf{N}(\tilde{\mathbb{I}} lck), pc_{\text{O}\tilde{\mathbf{W}}\mathbf{N}(\tilde{\mathbb{I}} lck)}) = [\text{halt}]^{pc_{\text{O}\tilde{\mathbf{W}}\mathbf{N}(\tilde{\mathbb{I}} lck)}))$ , given that  $\text{D}\tilde{\mathbf{L}}(\tilde{\mathbb{I}} lck)$  is a safe approximation of when  $lck$  must have been taken

by some thread in the corresponding concrete cases (c.f., Lemma 5.53), if any.

In the concrete case, a free (*unlocked*) lock is acquired as soon as some thread tries to do so (c.f., Tables 4.2 and 4.3 and Lemma 4.5). The purpose of DLLOCK, defined in Algorithm 5.11, is to derive a safe approximation of this point in time (Lemma 5.53). Note that Lemma 5.51 states that accumulating time for each thread individually is safe and that Lemma 5.52 states that the timing of a thread can be analyzed in isolation from all other threads.

**Lemma 5.51 (Time accumulation):**

Given the two configurations  $c@ \langle [T, pc_T, \mathbb{r}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$  and  $\tilde{c}@ \langle [T, pc_T^{\tilde{c}}, \tilde{\mathbb{r}}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \mathbf{Conf}$ , such that  $\mathbf{Thrd}_{\tilde{c}} \subseteq \mathbf{Thrd}$ , let  $\mathbf{Thrd}' = \{T \in \mathbf{Thrd}_{\tilde{c}} \mid t_T^a \in \gamma_t(\tilde{t}_T^a) \wedge pc_T = pc_T^{\tilde{c}}\}$ . Then  $\forall T \in \mathbf{Thrd}' : (t_T^a + \text{TIME}(c, T)) \in \gamma_t(\tilde{t}_T^a \dot{-}_t \text{ABSTIME}(\tilde{c}, T))$ .  $\square$

PROOF. Assume that the configurations  $c@ \langle [T, pc_T, \mathbb{r}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$  and  $\tilde{c}@ \langle [T, pc_T^{\tilde{c}}, \tilde{\mathbb{r}}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \mathbf{Conf}$  are such that  $\mathbf{Thrd}_{\tilde{c}} \subseteq \mathbf{Thrd}$ , and let  $\mathbf{Thrd}' = \{T \in \mathbf{Thrd}_{\tilde{c}} \mid t_T^a \in \gamma_t(\tilde{t}_T^a) \wedge pc_T = pc_T^{\tilde{c}}\}$ . Then, according to Assumption 5.50,  $\forall T \in \mathbf{Thrd}' : \text{TIME}(c, T) \in \gamma_t(\text{ABSTIME}(\tilde{c}, T))$ . Since  $\forall T \in \mathbf{Thrd}' : t_T^a \in \gamma_t(\tilde{t}_T^a)$ , it is easy to see that  $\forall T \in \mathbf{Thrd}' : (t_T^a + \text{TIME}(c, T)) \in \gamma_t(\tilde{t}_T^a \dot{-}_t \text{ABSTIME}(\tilde{c}, T))$ .  $\blacksquare$

**Lemma 5.52 (Thread isolation):**

Given the two configurations  $c^0@ \langle [T, pc_T^0, \mathbb{r}_T^0, t_T^{a0}]_{T \in \mathbf{Thrd}}, \mathbb{x}^0, \mathbb{l}^0 \rangle \in \mathbf{Conf}$  and  $\tilde{c}^0@ \langle [T, pc_T^{\tilde{c}^0}, \tilde{\mathbb{r}}_T^0, \tilde{t}_T^{a0}]_{T \in \mathbf{Thrd}_{\tilde{c}^0}}, \tilde{\mathbb{x}}^0, \tilde{\mathbb{l}}^0 \rangle \in \mathbf{Conf}$ , and some thread,  $T \in \mathbf{Thrd}_{\tilde{c}^0}$ , such that  $\mathbf{Thrd}_{\tilde{c}^0} \subseteq \mathbf{Thrd}$ ,  $t_T^{a0} \in \gamma_t(\tilde{t}_T^{a0})$  and  $pc_T^0 = pc_T^{\tilde{c}^0}$ , and some configuration  $c^{n+1}@ \langle [T, pc_T^{n+1}, \mathbb{r}_T^{n+1}, t_T^{a^{n+1}}]_{T \in \mathbf{Thrd}}, \mathbb{x}^{n+1}, \mathbb{l}^{n+1} \rangle$ , where

$$c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^1 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n+1}$$

for some  $n \geq 0$ ,

$$t_T^{a^{n+1}} \in \gamma_t(\tilde{t}_T^{a0} \dot{-}_t \text{ABSTIME}(\tilde{c}^0, T) \dot{-}_t \dots \dot{-}_t \text{ABSTIME}(\tilde{c}^n@ \langle [T, pc_T^{\tilde{c}^n}, \tilde{\mathbb{r}}_T^n, \tilde{t}_T^{an}]_{T \in \mathbf{Thrd}}, \tilde{\mathbb{x}}^n, \tilde{\mathbb{l}}^n \rangle, T))$$

given that  $\forall i \in \{1, \dots, n\} : \tilde{t}_T^{ai} = \tilde{t}_T^{a^{i-1}} \dot{-}_t \text{ABSTIME}(\tilde{c}^{i-1}, T)$ ,  $\forall i \in \{0, \dots, n\} : pc_T^i = pc_T^{\tilde{c}^i}$ ,  $\forall i \in \{0, \dots, n\} : T \in \mathbf{Thrd}_{\tilde{c}^i}^{\text{exe}}$ , and  $\forall c \in \{c^0, \dots, c^1, \dots, c^n\} \setminus \{c^0, c^1, \dots, c^n\} : T \notin \mathbf{Thrd}_{\tilde{c}^i}^{\text{exe}}$ , where  $\mathbf{Thrd}_{\tilde{c}^i}^{\text{exe}}$  and  $\mathbf{Thrd}_{\tilde{c}^i}^c$  are as defined in Table 4.3 for all  $\tilde{c}^i$  and all other  $c$  on the trace from  $c^0$  to  $c^{n+1}$ .  $\square$



PROOF. Assume that the configurations  $c^0 @ \langle [\mathbb{T}, pc_{\mathbb{T}}^0, \mathbb{T}^0, t_{\mathbb{T}}^{a^0}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{X}^0, \mathbb{I}^0 \rangle \in \mathbf{Conf}$  and  $\tilde{c}^0 @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}^0}, \tilde{\mathbb{T}}^0, \tilde{t}_{\mathbb{T}}^{a^0}]_{\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}^0}}, \tilde{\mathbb{X}}^0, \tilde{\mathbb{I}}^0 \rangle \in \mathbf{C\tilde{on}f}$ , and some thread,  $\mathbb{T} \in \mathbf{Thrd}$ , are such that  $\mathbf{Thrd}_{\tilde{c}^0} \subseteq \mathbf{Thrd}$ ,  $t_{\mathbb{T}}^{a^0} \in \gamma_i(\tilde{t}_{\mathbb{T}}^{a^0})$  and  $pc_{\mathbb{T}}^0 = pc_{\mathbb{T}}^{\tilde{c}^0}$ . Also assume that  $c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^1 \xrightarrow{prg} \dots \xrightarrow{prg} c^{n+1}$  for some configuration  $c^{n+1} @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{n+1}, \mathbb{T}^{n+1}, t_{\mathbb{T}}^{a^{n+1}}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{X}^{n+1}, \mathbb{I}^{n+1} \rangle$  and  $n \geq 0$ , for which  $\forall i \in \{0, \dots, n\} : \mathbb{T} \in \mathbf{Thrd}_{exe}^i$ , and  $\forall c \in \{c^0, \dots, c^1, \dots, c^n\} \setminus \{c^0, c^1, \dots, c^n\} : \mathbb{T} \notin \mathbf{Thrd}_{exe}^c$ , where  $\mathbf{Thrd}_{exe}^i$  and  $\mathbf{Thrd}_{exe}^c$  are as defined in Table 4.3 for all  $c^i$  and all other  $c$  on the trace from  $c^0$  to  $c^{n+1}$ .

From Table 4.3, it is easy to see that:

$$\begin{aligned} t_{\mathbb{T}}^{a^0} &= t_{\mathbb{T}}^{a^0} \\ t_{\mathbb{T}}^{a^1} &= t_{\mathbb{T}}^{a^0} + \text{TIME}(c^0, \mathbb{T}) \\ &\vdots \\ t_{\mathbb{T}}^{a^{n+1}} &= t_{\mathbb{T}}^{a^n} + \text{TIME}(c^n, \mathbb{T}) = \\ &\quad t_{\mathbb{T}}^{a^0} + \text{TIME}(c^0, \mathbb{T}) + \dots + \text{TIME}(c^n, \mathbb{T}) \end{aligned}$$

Let  $\{\tilde{c}^0, \dots, \tilde{c}^n @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}^i}, \tilde{\mathbb{T}}^i, \tilde{t}_{\mathbb{T}}^{a^i}]_{\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}^i}}, \tilde{\mathbb{X}}^i, \tilde{\mathbb{I}}^i \rangle\}$  be a set of some abstract configurations such that  $\tilde{c}^0$  has the properties assumed above,  $\forall i \in \{1, \dots, n\} : pc_{\mathbb{T}}^i = pc_{\mathbb{T}}^{\tilde{c}^i}$  and  $\forall i \in \{1, \dots, n\} : \tilde{t}_{\mathbb{T}}^{a^i} = \tilde{t}_{\mathbb{T}}^{a^{i-1}} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^{i-1}, \mathbb{T})$ . Then, according to Lemma 5.51:

$$\begin{aligned} (t_{\mathbb{T}}^{a^0} + \text{TIME}(c^0, \mathbb{T})) &\in \gamma_i(\tilde{t}_{\mathbb{T}}^{a^0} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^0, \mathbb{T})) \\ &\vdots \\ (t_{\mathbb{T}}^{a^n} + \text{TIME}(c^n, \mathbb{T})) &\in \gamma_i(\tilde{t}_{\mathbb{T}}^{a^n} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^n, \mathbb{T})) \end{aligned}$$

Since  $t_{\mathbb{T}}^{a^{n+1}} = t_{\mathbb{T}}^{a^n} + \text{TIME}(c^n, \mathbb{T})$ , this concludes the proof.  $\blacksquare$

**Lemma 5.53 (Soundness of DLLOCK):**

Given the valid concrete configurations (c.f., Definition 4.4), abstract configurations and lock

$$\begin{aligned} c^0 @ \langle [\mathbb{T}, pc_{\mathbb{T}}^0, \mathbb{T}^0, t_{\mathbb{T}}^{a^0}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{X}^0, \mathbb{I}^0 \rangle &\in \mathbf{Conf}, \\ c^m @ \langle [\mathbb{T}, pc_{\mathbb{T}}^m, \mathbb{T}^m, t_{\mathbb{T}}^{a^m}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{X}^m, \mathbb{I}^m \rangle &\in \mathbf{Conf}, \\ c^n @ \langle [\mathbb{T}, pc_{\mathbb{T}}^n, \mathbb{T}^n, t_{\mathbb{T}}^{a^n}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{X}^n, \mathbb{I}^n \rangle &\in \mathbf{Conf}, \\ \tilde{c}^0 @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}^0}, \tilde{\mathbb{T}}^0, \tilde{t}_{\mathbb{T}}^{a^0}]_{\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}^0}}, \tilde{\mathbb{X}}^0, \tilde{\mathbb{I}}^0 \rangle &\in \mathbf{C\tilde{on}f}, \\ \tilde{c}^j @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}^j}, \tilde{\mathbb{T}}^j, \tilde{t}_{\mathbb{T}}^{a^j}]_{\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}^j}}, \tilde{\mathbb{X}}^j, \tilde{\mathbb{I}}^j \rangle &\in \mathbf{C\tilde{on}f}, \text{ and} \\ lck &\in \mathbf{Lck}, \end{aligned}$$

such that

$$\begin{aligned}
 & 0 \leq m \leq n, \\
 & c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^m \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n, \\
 & 0 \leq j, \\
 & \mathbf{Thrd}_{\tilde{c}^j} \subseteq \mathbf{Thrd}_{\tilde{c}^0} \subseteq \mathbf{Thrd}, \\
 & \forall i \in \{m, \dots, n\} : \text{OWN}(\mathbb{1}^i \text{ lck}) = \perp_{\text{thrd}}, \\
 & \text{REL}(\mathbb{1}^m \text{ lck}) \in \gamma_t(\text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{1}}^j \text{ lck})), \\
 & \exists T \in \mathbf{Thrd}_{\tilde{c}^j} : (\text{STM}(T, pc_T^0) = [\text{lock lck}]^{pc_T^0} \wedge t_T^a \in \gamma_t(\tilde{t}_T^a) \wedge \tilde{t}_T^{a^j} = \tilde{t}_T^a \wedge \\
 & \quad pc_T^{\tilde{c}^j} = pc_T^{\tilde{c}^0} = pc_T^n = pc_T^0 \wedge T \in \mathbf{Thrd}_{\text{exe}}^{c^n} \wedge \\
 & \quad \forall i \in \{0, \dots, n\} : \text{OWN}(\mathbb{1}^i \text{ lck}) \neq T), \\
 & \forall i \in \{m, \dots, n-1\} : \forall T \in \mathbf{Thrd}_{\text{exe}}^{c^i} : \text{STM}(T, pc_T^i) \neq [\text{lock lck}]^{pc_T^i},
 \end{aligned}$$

where  $\mathbf{Thrd}_{\text{exe}}^{c^i}$  is as defined in Table 4.3 for  $c^i$ , DLLOCK satisfies:

$$\min(\{t_T^a + \text{TIME}(c^n, T) \mid T \in \mathbf{Thrd}\}) \in \gamma_t(\text{DLLOCK}(\tilde{c}^j, \text{lck})) \quad \square$$

PROOF. Given the valid concrete configurations (c.f., Definition 4.4), abstract configurations and lock

$$\begin{aligned}
 & c^0 @ \langle [T, pc_T^0, \mathbb{I}_T^0, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}^0, \mathbb{I}^0 \rangle \in \mathbf{Conf}, \\
 & c^m @ \langle [T, pc_T^m, \mathbb{I}_T^m, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}^m, \mathbb{I}^m \rangle \in \mathbf{Conf}, \\
 & c^n @ \langle [T, pc_T^n, \mathbb{I}_T^n, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}^n, \mathbb{I}^n \rangle \in \mathbf{Conf}, \\
 & \tilde{c}^0 @ \langle [T, pc_T^{\tilde{c}^0}, \tilde{\mathbb{I}}_T^0, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}^0}}, \tilde{\mathbb{x}}^0, \tilde{\mathbb{I}}^0 \rangle \in \mathbf{C\ddot{o}nf}, \\
 & \tilde{c}^j @ \langle [T, pc_T^{\tilde{c}^j}, \tilde{\mathbb{I}}_T^j, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}^j}}, \tilde{\mathbb{x}}^j, \tilde{\mathbb{I}}^j \rangle \in \mathbf{C\ddot{o}nf}, \text{ and} \\
 & \text{lck} \in \mathbf{Lck},
 \end{aligned}$$

are such that

$$\begin{aligned}
 & 0 \leq m \leq n, \\
 & c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^m \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n, \\
 & 0 \leq j, \\
 & \mathbf{Thrd}_{\tilde{c}^j} \subseteq \mathbf{Thrd}_{\tilde{c}^0} \subseteq \mathbf{Thrd}, \\
 & \forall i \in \{m, \dots, n\} : \text{OWN}(\mathbb{1}^i \text{ lck}) = \perp_{\text{thrd}}, \\
 & \text{REL}(\mathbb{1}^m \text{ lck}) \in \gamma_t(\text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{1}}^j \text{ lck})), \\
 & \exists T \in \mathbf{Thrd}_{\tilde{c}^j} : (\text{STM}(T, pc_T^0) = [\text{lock lck}]^{pc_T^0} \wedge t_T^a \in \gamma_t(\tilde{t}_T^a) \wedge \tilde{t}_T^{a^j} = \tilde{t}_T^a \wedge \\
 & \quad pc_T^{\tilde{c}^j} = pc_T^{\tilde{c}^0} = pc_T^n = pc_T^0 \wedge T \in \mathbf{Thrd}_{\text{exe}}^{c^n} \wedge \\
 & \quad \forall i \in \{0, \dots, n\} : \text{OWN}(\mathbb{1}^i \text{ lck}) \neq T), \\
 & \forall i \in \{m, \dots, n-1\} : \forall T \in \mathbf{Thrd}_{\text{exe}}^{c^i} : \text{STM}(T, pc_T^i) \neq [\text{lock lck}]^{pc_T^i},
 \end{aligned}$$

where  $\mathbf{Thrd}_{exe}^{c^i}$  is as defined in Table 4.3 for  $c^i$ . First note that:

- Since  $\forall i \in \{m, \dots, n-1\} : \forall T \in \mathbf{Thrd}_{exe}^{c^i} : (\text{STM}(T, pc_T^i) \neq [\text{lock } lck]^{pc_T^i} \wedge \text{OWN}(\mathbb{1}^i lck) = \perp_{\text{thrd}})$ , it must be that  $\text{REL}(\mathbb{1}^n lck) = \text{REL}(\mathbb{1}^m lck)$  (Tables 4.2 and 4.3).
- Since  $\forall i \in \{m, \dots, n\} : \text{OWN}(\mathbb{1}^i lck) = \perp_{\text{thrd}}$  and  $\text{REL}(\mathbb{1}^n lck) = \text{REL}(\mathbb{1}^m lck)$ , it must be that  $\forall T \in \mathbf{Thrd} : t_T^{a^m} \leq \text{REL}(\mathbb{1}^n lck)$  (Tables 4.2 and 4.3 and Lemma 4.2).
- Since time only moves forward (Lemma 4.2), it must be that for  $c^n$ ,  $\forall T \in \mathbf{Thrd} : \text{REL}(\mathbb{1}^n lck) \leq t_T^{a^n} + \text{TIME}(c^n, T)$ .
- Since  $\forall i \in \{m, \dots, n-1\} : \forall T \in \mathbf{Thrd}_{exe}^{c^i} : \text{STM}(T, pc_T^i) \neq [\text{lock } lck]^{pc_T^i}$ , it must be that  $\forall T \in \mathbf{Thrd} : (\text{STM}(T, pc_T^n) = [\text{lock } lck]^{pc_T^n} \Rightarrow t_T^{a^n} = t_T^{a^m})$  (Tables 4.2 and 4.3).
- Since  $\exists T \in \mathbf{Thrd}_{\tilde{c}^j} : (\text{STM}(T, pc_T^0) = [\text{lock } lck]^{pc_T^0} \wedge t_T^{a^0} \in \gamma_t(\tilde{t}_T^{a^0}) \wedge \tilde{t}_T^{a^j} = \tilde{t}_T^{a^0} \wedge pc_T^{\tilde{c}^j} = pc_T^{c^0} = pc_T^n = pc_T^0 \wedge T \in \mathbf{Thrd}_{exe}^{c^n} \wedge \forall i \in \{0, \dots, n\} : \text{OWN}(\mathbb{1}^i lck) \neq T)$ ,  $\mathbf{Thrd}_{\tilde{c}^j} \subseteq \mathbf{Thrd}$ ,  $\forall T \in \mathbf{Thrd} : t_T^{a^m} \leq \text{REL}(\mathbb{1}^n lck)$ ,  $\forall T \in \mathbf{Thrd} : \text{REL}(\mathbb{1}^n lck) \leq t_T^{a^n} + \text{TIME}(c^n, T)$  and  $\forall T \in \mathbf{Thrd} : (\text{STM}(T, pc_T^n) = [\text{lock } lck]^{pc_T^n} \Rightarrow t_T^{a^n} = t_T^{a^m})$  it must be that  $\exists T \in \mathbf{Thrd}_{\tilde{c}^j} : t_T^{a^m} \leq \text{REL}(\mathbb{1}^n lck) \leq t_T^{a^m} + \text{TIME}(c^n, T) \wedge \text{STM}(T, pc_T^n) = [\text{lock } lck]^{pc_T^n} \wedge t_T^{a^0} \in \gamma_t(\tilde{t}_T^{a^0}) \wedge \tilde{t}_T^{a^j} = \tilde{t}_T^{a^0} \wedge pc_T^{\tilde{c}^j} = pc_T^{c^0} = pc_T^n = pc_T^0 \wedge T \in \mathbf{Thrd}_{exe}^{c^n} \wedge \forall i \in \{0, \dots, n\} : \text{OWN}(\mathbb{1}^i lck) \neq T)$ .

From here on, it will be assumed that  $T' \in \mathbf{Thrd}_{\tilde{c}^j}$  is one of the threads such that  $\text{STM}(T', pc_{T'}^0) = [\text{lock } lck]^{pc_{T'}^0} \wedge t_{T'}^{a^m} \leq \text{REL}(\mathbb{1}^n lck) \leq t_{T'}^{a^n} + \text{TIME}(c^n, T') \wedge t_{T'}^{a^0} \in \gamma_t(\tilde{t}_{T'}^{a^0}) \wedge \tilde{t}_{T'}^{a^j} = \tilde{t}_{T'}^{a^0} \wedge pc_{T'}^{\tilde{c}^j} = pc_{T'}^{c^0} = pc_{T'}^n = pc_{T'}^0 \wedge T' \in \mathbf{Thrd}_{exe}^{c^n} \wedge \forall i \in \{0, \dots, n\} : \text{OWN}(\mathbb{1}^i lck) \neq T')$ .

- Let  $\{m_1, \dots, m_2\}$  be the set of indices, such that  $0 \leq m_1 \leq m_2 < m$ ,  $\forall i \in \{m_1, \dots, m_2\} : T' \in \mathbf{Thrd}_{exe}^{c^i}$  and  $\forall i \in \{0, \dots, m\} \setminus \{m_1, \dots, m_2\} : T' \notin \mathbf{Thrd}_{exe}^{c^i}$ , where  $\mathbf{Thrd}_{exe}^{c^i}$  is as defined in Table 4.3 for  $c^i$  (note that it is possible that  $\{m_1, \dots, m_2\} = \emptyset$ ; it should also be noted that  $T' \notin \mathbf{Thrd}_{exe}^{c^m}$ ). Since  $\mathbf{Thrd}_{\tilde{c}^j} \subseteq \mathbf{Thrd}$ ,  $t_{T'}^{a^0} \in \gamma_t(\tilde{t}_{T'}^{a^0})$ ,  $\tilde{t}_{T'}^{a^j} = \tilde{t}_{T'}^{a^0}$ ,  $c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^m$  and  $0 \leq m$ , it is easy to see that every configuration,  $\tilde{c}'$ , created by the **repeat**-loop within  $\text{DLLOCK}(\tilde{c}^j, lck)$  fulfills the assumptions of

Lemma 5.52. Furthermore, it is easy to see that (according to Lemma 5.52)

$$t_{T'}^{a^m} \in \gamma_t(\tilde{t}_{T'}^{a^0} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^{m_1}, T') \tilde{\vdash}_t \dots \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^{m_2}, T'))$$

where  $\tilde{c}^{m_1}, \dots, \tilde{c}^{m_2}$  correspond to a  $\tilde{c}'$  derived by the **repeat**-loop (in total, there are  $|\{m_1, \dots, m_2\}|$   $\tilde{c}'$ -configurations for the expression above).

For the sake of readability, let

$$\begin{aligned} \tilde{t}_{T'}^{a''} &= \tilde{t}_{T'}^{a^0} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^{m_1}, T') \tilde{\vdash}_t \dots \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^{m_2}, T') \\ \tilde{c}'' &= \langle [T, pc_T, \tilde{\pi}_T, (T = T' ? \tilde{t}_{T'}^{a''} : \tilde{t}_{T'}^{a^j})]_{T \in \mathbf{Thrd}_{\tilde{c}'}, \tilde{\mathbb{X}}, \tilde{\mathbb{I}}} \rangle \end{aligned}$$

where  $\tilde{c}^{m_1}, \dots, \tilde{c}^{m_2}$  are defined as in the bullet above.

Assuming that  $\tilde{t}_{dl}$  is safe at the start of each iteration of the **for all**  $T \in \mathbf{Thrd}_{\tilde{c}'}$ -loop, where  $T$  is such that  $\text{STM}(T, pc_T^n) = [\text{lock } lck]^{pc_T^n}$ , it should be shown that  $\min(\{t_{T'}^{a''} + \text{TIME}(c^n, T) \mid T \in \mathbf{Thrd}_{\tilde{c}'}\}) \in \gamma_t(\tilde{t}_{dl})$  is always fulfilled at the end of each loop-iteration. It is easy to see that the initial value of  $\tilde{t}_{dl}$  (i.e.,  $\tilde{t}_t$ ) is trivially safe since  $\forall T \in \mathbf{Thrd}_{\tilde{c}'} : t_{T'}^{a''} + \text{TIME}(c^n, T) \in \gamma_t(\tilde{t}_t)$ . Note that  $\forall c \in \mathbf{Conf} : \forall T \in \mathbf{Thrd} : \text{TIME}(c, T) \geq 0$  (Assumption 4.1). Several cases need to be considered.

1. If  $\text{TIME}(c^n, T') = 0$ , then  $t_{T'}^{a''} + \text{TIME}(c^n, T') = t_{T'}^{a''} = \text{REL}(\mathbb{I}^n lck)$  (remember that  $t_{T'}^{a''} = t_{T'}^{a^m}$  and  $\text{REL}(\mathbb{I}^n lck) = \text{REL}(\mathbb{I}^m lck)$ ) and  $0 \in \text{ABSTIME}(\tilde{c}'', T')$  (Assumption 5.50). Since  $0 \in \gamma_t(\text{ABSTIME}(\tilde{c}'', T'))$ , it will not be possible to determine a  $\tilde{t}_{T'}^{a''}$  such that  $\text{R}\tilde{\text{E}}\text{L}(\tilde{\mathbb{I}}^j lck) \lesssim_t \tilde{t}_{T'}^{a''}$ . However, for the iteration of the **repeat**-loop for which  $0 \in \text{ABSTIME}(\tilde{c}'', T')$ , it must be that  $\text{R}\tilde{\text{E}}\text{L}(\tilde{\mathbb{I}}^j lck) \not\lesssim_t \tilde{t}_{T'}^{a''}$ .  $\text{R}\tilde{\text{E}}\text{L}(\tilde{\mathbb{I}}^j lck)$  provides a safe base for when  $T'$  would acquire  $lck$  since  $\text{REL}(\mathbb{I}^n lck) \in \gamma_t(\text{R}\tilde{\text{E}}\text{L}(\tilde{\mathbb{I}}^j lck))$ . Thus, according to Assumption 5.50, it must be that  $(t_{T'}^{a''} + \text{TIME}(c^n, T')) \in \gamma_t((\tilde{t} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}''', T')) \sqcup_t \alpha_t(\{-\infty\}))$ , where  $\tilde{c}''' = \langle [T, pc_T, \tilde{\pi}_T, (T = T' ? \tilde{t} : \tilde{t}_{T'}^{a^j})]_{T \in \mathbf{Thrd}_{\tilde{c}'}, \tilde{\mathbb{X}}, \tilde{\mathbb{I}}} \rangle$  and  $\tilde{t} = \tilde{t}_{T'}^{a''} \sqcup_t \text{R}\tilde{\text{E}}\text{L}(\tilde{\mathbb{I}}^j lck)$ . But then, it is easy to see that  $\min(\{t_{T'}^{a''} + \text{TIME}(c^n, T) \mid T \in \mathbf{Thrd}_{\tilde{c}'}\}) \in \gamma_t((\tilde{t} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}''', T')) \sqcup_t \alpha_t(\{-\infty\})) \sqcap_t \tilde{t}_{dl}$ .
2. If  $\text{TIME}(c^n, T') > 0$ , then two cases must be considered.
  - (a) If  $0 \in \gamma_t(\text{ABSTIME}(\tilde{c}'', T'))$  (or for any  $\tilde{c}'$  of the **repeat**-loop), it will not be possible to determine a  $\tilde{t}_{T'}^{a''}$  such that  $\text{R}\tilde{\text{E}}\text{L}(\tilde{\mathbb{I}}^j lck) \lesssim_t \tilde{t}_{T'}^{a''}$ . However, this proof is the same as that of 1 above.

- (b) If  $0 \notin \gamma_t(\text{ABSTIME}(\tilde{c}'', T'))$  (as well as for all  $\tilde{c}'$  of the **repeat-loop**), then a  $\tilde{t}_{T'}^{a'}$  such that  $\text{REL}(\tilde{\mathbb{I}}^j lck) \tilde{z}_t \tilde{t}_{T'}^{a'}$  can be derived. Since  $t_{T'}^{a''} \leq \text{REL}(\mathbb{I}^n lck)$ ,  $\text{REL}(\mathbb{I}^n lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}^j lck))$  and  $t_{T'}^{a''} \in \gamma_t(\tilde{t}_{T'}^{a''})$ , it must be that  $\text{REL}(\tilde{\mathbb{I}}^j lck) \tilde{z}_t \tilde{t}_{T'}^{a''}$ , and thus, the **repeat-loop** will iterate *at least* once more when  $\tilde{t}_{T'}^{a'} = \tilde{t}_{T'}^{a''}$ . Since  $\text{REL}(\mathbb{I}^n lck) < t_{T'}^{a''} + \text{TIME}(c^n, T')$ , it must be that (since  $t_{T'}^{a''} = t_{T'}^{a''}$ )  $t_{T'}^{a''} + \text{TIME}(c^n, T) \in \gamma_t(\tilde{t}_{T'}^{a''} \dot{+}_t \text{ABSTIME}(\tilde{c}'', T'))$ . Thus,  $t_{T'}^{a''} + \text{TIME}(c^n, T) \in \gamma_t(\tilde{t}_{T'}^{a''} \sqcup_t \alpha_t(\{-\infty\}))$ , where  $\tilde{t}_{T'}^{a'}$  and  $\tilde{c}'$  are derived from  $\tilde{c}''$  by the **repeat-loop**, and thus  $\max(\gamma_t(\tilde{t}_{T'}^{a''})) \leq \max(\gamma_t(\tilde{t}_{T'}^{a'}))$  (c.f., Assumption 5.50). But then, it is easy to see that  $\min(\{t_{T'}^{a''} + \text{TIME}(c^n, T) \mid T \in \mathbf{Thrd}_\varepsilon\}) \in \gamma_t((\tilde{t}_{T'}^{a''} \sqcup_t \alpha_t(\{-\infty\})) \dot{\sqcap}_t \tilde{t}_{dl})$ .

Thus, it must be that:

$$\min(\{t_{T'}^{a''} + \text{TIME}(c^n, T) \mid T \in \mathbf{Thrd}\}) \in \gamma_t(\text{DLLOCK}(\tilde{c}^j, lck)) \quad \blacksquare$$

The accumulated time,  $\tilde{t}_{T'}^{a'} \in \mathbf{Time}$ , for a thread,  $T \in \mathbf{Thrd}_\varepsilon$ , is determined using  $\text{ACCTIME}$ , defined in Algorithm 5.12, which is partially a safe approximation of the concrete accumulated time of  $T$  (Lemma 5.54). This is because the way that time accumulates for threads executing `lock lck` for some lock,  $lck \in \mathbf{Lck}$ , that is currently acquired by some other thread differs in the concrete and abstract semantics. In the concrete semantics, the `lock`-statement is just considered to finish its execution, without successfully acquiring  $lck$ , after the (relative) time given by  $\text{TIME}$ , then a new instance of the same `lock`-statement is executed (c.f., Tables 4.2 and 4.3); i.e., the thread is actively spinning on the lock.

In the abstract semantics (c.f., Tables 5.5 and 5.6 and Algorithms 5.11 and 5.12), a thread issuing `lock lck` for some lock,  $lck \in \mathbf{Lck}$ , that is currently acquired by some other thread would be frozen until it is assigned  $lck$ , if this ever occurs; i.e., the thread's accumulated time would not be increased while it is waiting to be assigned  $lck$ . When (and if) the thread is later assigned  $lck$ , its accumulated execution time is advanced based on when  $lck$  became free (*unlocked*).

If the lock,  $lck \in \mathbf{Lck}$ , is not currently assigned to some other thread when some thread issues `lock lck`, the behavior is the same in both the concrete and abstract semantics in case the `lock`-issuing thread successfully acquires  $lck$ ; i.e., the thread's execution time will be accumulated based on  $\text{TIME}$  and  $\text{ABSTIME}$ , respectively.

NOTE. `ACCTIME` is not directly safe for the case that  $\text{STM}(\mathbb{T}, pc_{\mathbb{T}}) = [\text{lock } lck]^{pc_{\mathbb{T}}} \wedge \text{OWN}(\mathbb{I}'' lck) \neq \mathbb{T}$ . In the concrete case,  $\mathbb{T}$  will be executed in a spin-lock fashion, while in the corresponding abstract case,  $\mathbb{T}$  will be frozen (i.e., its accumulated time will not be updated). This case is further considered in the proof of Lemma 5.57.

`ACCTIME` is also not directly safe for the case that  $\mathbb{T}$  has been waiting but is now assigned *lck*, i.e., a catchup will be performed in the abstract case, since there could be an extra abstract configuration such that  $\tilde{t}_{\mathbb{T}}^a \prec_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}'', lck)$  and  $\tilde{t}_{\mathbb{T}}^a \dagger_t \text{ABS}\text{TIME}(\tilde{c}^0, \mathbb{T}) \not\prec_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}'', lck)$ . This case is also further considered in the proof of Lemma 5.57.

**Lemma 5.54 (Partial soundness of `ACCTIME`):**

Given the valid concrete configuration  $c@ \langle [\mathbb{T}', pc_{\mathbb{T}'}, \mathbb{R}_{\mathbb{T}'}, t_{\mathbb{T}'}^a]_{\mathbb{T}' \in \mathbf{Thrd}}, \mathbb{X}, \mathbb{I} \rangle \in$

**Conf** (c.f., Definition 4.4), the abstract configuration  $\tilde{c}^0@ \langle [\mathbb{T}', pc_{\mathbb{T}'}, \tilde{\mathbb{R}}_{\mathbb{T}'}, \tilde{t}_{\mathbb{T}'}^a]_{\mathbb{T}' \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbb{X}}, \tilde{\mathbb{I}} \rangle \in \mathbf{C}\ddot{\text{O}}\mathbf{n}\mathbf{f}$ , and some thread,  $\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}}$ , such that

$$\begin{aligned} & \mathbf{Thrd}_{\tilde{c}} \subseteq \mathbf{Thrd} \wedge \\ & pc_{\mathbb{T}} = pc_{\mathbb{T}}^{\tilde{c}} \wedge \\ & t_{\mathbb{T}}^a \in \gamma_t(\tilde{t}_{\mathbb{T}}^a) \wedge \\ & (\mathbb{T} \in \mathbf{Thrd}_{exe}^c \wedge \forall lck \in \mathbf{Lck} : (\text{STM}(\mathbb{T}, pc_{\mathbb{T}}) = [\text{lock } lck]^{pc_{\mathbb{T}}} \Rightarrow \\ & \quad (\text{OWN}(\tilde{\mathbb{I}}'' lck) = \mathbb{T} \wedge \text{OWN}(\mathbb{I}'' lck) = \mathbb{T})) \iff \mathbb{T} \in \mathbf{Thrd}_{exe}^{\tilde{c}} \wedge \\ & \forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{I}'' lck) = \mathbb{T} \Rightarrow (\text{OWN}(\tilde{\mathbb{I}}'' lck) = \text{OWN}(\mathbb{I}'' lck) \wedge \\ & \quad \text{DL}(\mathbb{I}'' lck) \in \gamma_t(\tilde{\text{D}}\ddot{\text{L}}(\tilde{\mathbb{I}}'' lck)) \wedge \\ & \quad \text{POWN}(\mathbb{I}'' lck) = \text{POWN}(\tilde{\mathbb{I}}'' lck) \wedge \\ & \quad \text{REL}(\mathbb{I}'' lck) \in \gamma_t(\text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}'' lck)) \wedge \\ & \quad \min(\gamma_t(\tilde{\text{D}}\ddot{\text{L}}(\tilde{\mathbb{I}}'' lck))) = -\infty)), \end{aligned}$$

where  $\mathbf{Thrd}_{exe}^c$  and  $\mathbb{I}''$ , and  $\mathbf{Thrd}_{exe}^{\tilde{c}}$  and  $\tilde{\mathbb{I}}''$ , are as defined in Tables 4.3 and 5.6, respectively,

$$t_{\mathbb{T}}^a \in \gamma_t(\text{ACCTIME}(\langle [\mathbb{T}', pc_{\mathbb{T}'}, \tilde{\mathbb{R}}_{\mathbb{T}'}, \tilde{t}_{\mathbb{T}'}^a]_{\mathbb{T}' \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbb{X}}, \tilde{\mathbb{I}}'' \rangle, \mathbf{Thrd}_{exe}^{\tilde{c}}, \mathbb{T}))$$

where  $t_{\mathbb{T}}^a$  is as defined in Table 4.3. □

PROOF. Assume that the (valid; c.f., Definition 4.4) configurations  $c@ \langle [\mathbb{T}', pc_{\mathbb{T}'}, \mathbb{R}_{\mathbb{T}'}, t_{\mathbb{T}'}^a]_{\mathbb{T}' \in \mathbf{Thrd}}, \mathbb{X}, \mathbb{I} \rangle \in \mathbf{Conf}$  and  $\tilde{c}^0@ \langle [\mathbb{T}', pc_{\mathbb{T}'}, \tilde{\mathbb{R}}_{\mathbb{T}'}, \tilde{t}_{\mathbb{T}'}^a]_{\mathbb{T}' \in \mathbf{Thrd}_{\tilde{c}}},$

$\tilde{x}, \tilde{l}$   $\in$  **Cõnf** and the thread  $T \in \mathbf{Thrd}_{\tilde{c}}$  are such that

$$\begin{aligned}
 & \mathbf{Thrd}_{\tilde{c}} \subseteq \mathbf{Thrd} \wedge \\
 & pc_T = pc_T^{\tilde{c}} \wedge \\
 & t_T^a \in \gamma_t(\tilde{t}_T^a) \wedge \\
 & (T \in \mathbf{Thrd}_{exe}^c \wedge \forall lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \Rightarrow \\
 & \quad (\text{O}\tilde{\text{W}}\text{N}(\tilde{l}'' lck) = T \wedge \text{OWN}(\tilde{l}'' lck) = T))) \iff T \in \mathbf{Thrd}_{exe}^{\tilde{c}} \wedge \\
 & \forall lck \in \mathbf{Lck} : (\text{OWN}(\tilde{l}'' lck) = T \Rightarrow (\text{OWN}(\tilde{l}'' lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{l}'' lck) \wedge \\
 & \quad \text{DL}(\tilde{l}'' lck) \in \gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{l}'' lck)) \wedge \\
 & \quad \text{PO}\tilde{\text{W}}\text{N}(\tilde{l}'' lck) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{l}'' lck) \wedge \\
 & \quad \text{REL}(\tilde{l}'' lck) \in \gamma_t(\tilde{\text{R}}\tilde{\text{E}}\tilde{\text{L}}(\tilde{l}'' lck)) \wedge \\
 & \quad \min(\gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{l}'' lck))) = -\infty)),
 \end{aligned}$$

where  $\mathbf{Thrd}_{exe}^c$  and  $\tilde{l}''$ , and  $\mathbf{Thrd}_{exe}^{\tilde{c}}$  and  $\tilde{l}''$ , are as defined in Tables 4.3 and 5.6, respectively.

For the sake of readability, let  $\tilde{c} = \langle [T', pc_{T'}^{\tilde{c}}, \tilde{t}_{T'}^a, \tilde{t}_T^a]_{T' \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l}'' \rangle$  when considering the following cases. Note that **Time** = **Intv**.

1. If  $T \notin \mathbf{Thrd}_{exe}^c$  (and thus,  $T \notin \mathbf{Thrd}_{exe}^{\tilde{c}}$ ), then  $t_T^a = t_T^a$  (Table 4.3) and  $\text{ACCTIME}(\tilde{c}, \mathbf{Thrd}_{exe}^{\tilde{c}}, T) = \tilde{t}_T^a$ . Thus,  $t_T^a \in \gamma_t(\text{ACCTIME}(\tilde{c}, \mathbf{Thrd}_{exe}^{\tilde{c}}, T))$ .
2. If  $T \in \mathbf{Thrd}_{exe}^c$  and for some  $a \in \mathbf{Aexp}$ ,  $b \in \mathbf{Bexp}$ ,  $l \in \mathbf{Lbl}_T$ ,  $r \in \mathbf{Reg}_T$ ,  $x \in \mathbf{Var}$  and  $lck \in \mathbf{Lck}$ ,  $\text{STM}(T, pc_T) \in \{[\text{skip}]^{pc_T}, [r := a]^{pc_T}, [\text{if } b \text{ goto } l]^{pc_T}, [\text{store } r \text{ to } x]^{pc_T}, [\text{load } r \text{ from } x]^{pc_T}, [\text{unlock } lck]^{pc_T}\}$ , i.e.,  $\forall lck' \in \mathbf{Lck} : \text{STM}(T, pc_T) \neq [\text{lock } lck']^{pc_T}$  (and thus,  $T \in \mathbf{Thrd}_{exe}^{\tilde{c}}$  since  $(T \in \mathbf{Thrd}_{exe}^c \wedge \forall lck' \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck']^{pc_T} \Rightarrow (\text{O}\tilde{\text{W}}\text{N}(\tilde{l}'' lck') = T \wedge \text{OWN}(\tilde{l}'' lck') = T)))) \iff T \in \mathbf{Thrd}_{exe}^{\tilde{c}}$ , then  $\text{ACCTIME}(\tilde{c}, \mathbf{Thrd}_{exe}^{\tilde{c}}, T) = \tilde{t}_T^a \uparrow_t \text{ABSTIME}(\tilde{c}, T)$  and by Table 4.3,  $t_T^a = t_T^a + \text{TIME}(c, T)$ . Thus, by Lemma 5.51,  $t_T^a \in \gamma_t(\text{ACCTIME}(\tilde{c}, \mathbf{Thrd}_{exe}^{\tilde{c}}, T))$ .
3. If  $T \in \mathbf{Thrd}_{exe}^c$  and for some  $lck \in \mathbf{Lck}$ ,  $\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T}$  and  $\text{OWN}(\tilde{l}'' lck) = T$ , and thus,  $T \in \mathbf{Thrd}_{exe}^{\tilde{c}}$  since  $(T \in \mathbf{Thrd}_{exe}^c \wedge \forall lck' \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck']^{pc_T} \Rightarrow (\text{O}\tilde{\text{W}}\text{N}(\tilde{l}'' lck') = T \wedge \text{OWN}(\tilde{l}'' lck') = T)))) \iff T \in \mathbf{Thrd}_{exe}^{\tilde{c}}$ , then several cases need to be considered. Note that  $\min(\gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{l}'' lck))) = -\infty$ , since  $\forall lck' \in \mathbf{Lck} : (\text{OWN}(\tilde{l}'' lck') = T \Rightarrow \min(\gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{l}'' lck'))) = -\infty)$  and  $\text{OWN}(\tilde{l}'' lck) = T$ , and that  $T$  cannot acquire  $lck$  at any time,  $\tilde{t}$ , such that  $\tilde{t} \prec_t \text{REL}(\tilde{l}'' lck)$ , since  $lck$  has not been released at  $\tilde{t}$ , or  $\tilde{\text{D}}\tilde{\text{L}}(\tilde{l}'' lck) \prec_t \tilde{t}$ , since by then some other thread would have taken  $lck$  (c.f., Tables 5.5 and 5.6).

- (a) If  $s\tilde{T}T(\tilde{l}'' lck) = \text{locked}$  (and  $STT(\tilde{l}'' lck) = \text{locked}$  since  $c$  is valid and  $\text{OWN}(\tilde{l}'' lck) \neq \perp_{\text{thrd}}$ ), then  $t_T^{\text{all}} = t_T^a + \text{TIME}(c, T)$  and  $\text{ACCTIME}(\tilde{c}, \mathbf{Thrd}_{\text{exe}}^{\tilde{c}}, T) = \tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T)$ . Thus,  $t_T^{\text{all}} \in \gamma_t(\text{ACCTIME}(\tilde{c}, \mathbf{Thrd}_{\text{exe}}^{\tilde{c}}, T))$  (Lemma 5.51).
- (b) Assume that  $s\tilde{T}T(\tilde{l}'' lck) = \text{unlocked} \wedge \tilde{D}\tilde{L}(\tilde{l}'' lck) \lesssim_t (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T))$ . Then, in the concrete case, it must be that  $T$  cannot be the thread acquiring  $lck$  since  $\text{DL}(\tilde{l}'' lck) \in \gamma_t(\tilde{D}\tilde{L}(\tilde{l}'' lck))$ ,  $t_T^a \in \gamma_t(\tilde{t}_T^a)$ ,  $\text{TIME}(c, T) \in \gamma_t(\text{ABSTIME}(\tilde{c}, T))$  and  $t_T^a + \text{TIME}(c, T) = \text{DL}(\tilde{l}'' lck)$  whenever  $T$  acquires  $lck$  (Tables 4.2 and 4.3). But, then it cannot be that  $s\tilde{T}T(\tilde{l}'' lck) = \text{unlocked} \wedge \tilde{D}\tilde{L}(\tilde{l}'' lck) \lesssim_t (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T))$  since in the concrete case,  $T$  does successfully acquire  $lck$ , which means that the corresponding branch cannot apply for the given case. (Note that such a  $\tilde{c}$  will not be further considered; c.f., Algorithm 6.6 and Tables 5.5 and 5.6.)
- (c) Note that the  $s\tilde{T}T(\tilde{l}'' lck) = \text{unlocked} \wedge \tilde{D}\tilde{L}(\tilde{l}'' lck) \not\lesssim_t (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T)) \wedge (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T)) \lesssim_t \text{R}\tilde{E}\tilde{L}(\tilde{l}'' lck)$  conditioned branch, which applies to cases where  $T$  has been frozen for sure while waiting to acquire  $lck$  but has now been assigned  $lck$ , cannot be taken either. To see this, note that since  $c$  is valid, it must be that  $\text{REL}(\tilde{l}'' lck) \leq t_T^a + \text{TIME}(c, T)$  (Definition 4.4). Then, since  $t_T^a \in \gamma_t(\tilde{t}_T^a)$ ,  $\text{TIME}(c, T) \in \gamma_t(\text{ABSTIME}(\tilde{c}^0, T))$  (c.f., Assumption 5.50),  $\text{OWN}(\tilde{l}'' lck) = T$  and  $\text{OWN}(\tilde{l}'' lck) = T \Rightarrow \text{REL}(\tilde{l}'' lck) \in \gamma_t(\text{R}\tilde{E}\tilde{L}(\tilde{l}'' lck))$ , it must be that  $\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}^0, T) \not\lesssim_t \text{R}\tilde{E}\tilde{L}(\tilde{l}'' lck)$ . This branch is further considered when the freezing of threads is proven to be safe (c.f., the proof of Lemma 5.57).
- (d) If  $s\tilde{T}T(\tilde{l}'' lck) = \text{unlocked} \wedge \tilde{D}\tilde{L}(\tilde{l}'' lck) \not\lesssim_t (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T)) \wedge (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T)) \not\lesssim_t \text{R}\tilde{E}\tilde{L}(\tilde{l}'' lck) \wedge (\text{PO}\tilde{W}\tilde{N}(\tilde{l}'' lck) = T \vee \text{R}\tilde{E}\tilde{L}(\tilde{l}'' lck) \lesssim_t (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T)))$ , then two cases must be considered.
- i. If  $\text{PO}\tilde{W}\tilde{N}(\tilde{l}'' lck) = T$ , then the sequential execution of the statements of a thread (c.f., Tables 4.2 and 4.3) gives that  $T$  must acquire  $lck$  at  $\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T)$ , but not at a point in time,  $\tilde{t}$ , such that  $\tilde{D}\tilde{L}(\tilde{l}'' lck) \lesssim_t \tilde{t}$ , because by then, some other thread must have already acquired  $lck$  (since  $\text{DL}(\tilde{l}'' lck) \in \gamma_t(\tilde{D}\tilde{L}(\tilde{l}'' lck))$ ). Thus, it must be that  $t_T^{\text{all}} \in \gamma_t((\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T)) \sqcap_t \tilde{D}\tilde{L}(\tilde{l}'' lck))$ .
  - ii. If  $\text{R}\tilde{E}\tilde{L}(\tilde{l}'' lck) \lesssim_t (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T))$ , then Lemma 5.51



gives that  $t_T^{al} \in \gamma_t((\tilde{i}_T^a \dot{\dashv} \text{ABSTIME}(\tilde{c}, T)) \dot{\dashv} \text{DL}(\tilde{\mathbb{I}}'' lck))$   
 since  $t_T^{al} = \text{DL}(\mathbb{I}'' lck)$  (c.f., Tables 4.2 and 4.3),  $\text{DL}(\mathbb{I}'' lck) \in$   
 $\gamma_t(\text{DL}(\tilde{\mathbb{I}}'' lck))$  and  $\text{REL}(\mathbb{I}'' lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}'' lck))$ .

- (e) If  $\text{S}\dot{\dashv}\text{T}(\tilde{\mathbb{I}}'' lck) = \text{unlocked} \wedge \text{DL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} (\tilde{i}_T^a \dot{\dashv} \text{ABSTIME}(\tilde{c}, T)) \wedge$   
 $(\tilde{i}_T^a \dot{\dashv} \text{ABSTIME}(\tilde{c}, T)) \dot{\dashv} \text{REL}(\tilde{\mathbb{I}}'' lck) \neq \perp \wedge T \neq \text{PO\dot{W}N}(\tilde{\mathbb{I}}'' lck)$ ,  
 then let  $\tilde{i}_T^{all} = \tilde{i}_T^a \dot{\dashv} \text{ABSTIME}(\tilde{c}, T)$ , which is obviously a safe ap-  
 proximation of the first point in time at which T can acquire  $lck$ .  
 Also let  $\tilde{c}'$  be any configuration derived before (i.e.,  $\tilde{c}' = \tilde{c}$ ) or inside  
 the **repeat**-loop. Note that  $\tilde{i}_T^i = \tilde{i}_T^i$  is used to exit the loop in case  
 $\text{DL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} (\tilde{i}_T^a \dot{\dashv} \text{ABSTIME}(\tilde{c}', T))$  or  $0 \in \gamma_t(\text{ABSTIME}(\tilde{c}', T))$ ,  
 where the latter case means that a  $\tilde{i}_T^{al}$  such that  $\text{REL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} \tilde{i}_T^{al}$   
 cannot be derived.
- i. If  $\text{DL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} \tilde{i}_T^{al} \dot{\dashv} \text{ABSTIME}(\tilde{c}', T)$ , then it must be that at  
 $\tilde{i}_T^{al} \dot{\dashv} \text{ABSTIME}(\tilde{c}', T)$ , some other thread will have acquired  
 $lck$  (hence,  $\tilde{i}_T^{al}$  is the last point in time when T can acquire  
 $lck$ ). Thus, it must be that  $t_T^{al} \in \gamma_t((\tilde{i}_T^{all} \dot{\dashv} \tilde{i}_T^{al}) \dot{\dashv} \text{DL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv}$   
 $(\text{REL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} \alpha_t(\{\infty\})))$  since  $\text{DL}(\mathbb{I}'' lck) \in \gamma_t(\text{DL}(\tilde{\mathbb{I}}'' lck))$   
 and  $\text{REL}(\mathbb{I}'' lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}'' lck))$ .
  - ii. If  $0 \in \gamma_t(\text{ABSTIME}(\tilde{c}', T))$  and also  $\text{DL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} \tilde{i}_T^{al} \dot{\dashv}$   
 $\text{ABSTIME}(\tilde{c}', T)$ , then it must be that  $\tilde{i} \dot{\dashv} \text{ABSTIME}(\tilde{c}'', T)$ , where  $\tilde{i} =$   
 $(\tilde{i}_T^{all} \dot{\dashv} \alpha_t(\{\infty\})) \dot{\dashv} \text{REL}(\tilde{\mathbb{I}} lck)$  and  $\tilde{c}'' = \langle [\text{T}', pc_{\text{T}'}, \mathbb{I}_{\text{T}'}, (\text{T} = \text{T}' ? \tilde{i} : \tilde{i}_T^a)]_{\text{T}' \in \text{Thrd}_{\tilde{c}}}, \mathbb{S}, \tilde{\mathbb{I}}'' \rangle$ ,  
 is a safe approximation of the last point in time when T  
 can (or rather, will) acquire  $lck$  (c.f., Assumption 5.50)  
 since  $\text{REL}(\mathbb{I}'' lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}'' lck))$ . Thus, it must be that  
 $t_T^{al} \in \gamma_t((\tilde{i}_T^{all} \dot{\dashv} \tilde{i}_T^{al}) \dot{\dashv} \text{DL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} (\text{REL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} \alpha_t(\{\infty\})))$   
 since  $\text{REL}(\mathbb{I}'' lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}'' lck))$  and  $\text{DL}(\mathbb{I}'' lck) \in$   
 $\gamma_t(\text{DL}(\tilde{\mathbb{I}}'' lck))$ .
  - iii. If  $0 \notin \gamma_t(\text{ABSTIME}(\tilde{c}', T))$  and also  $\text{DL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} \tilde{i}_T^{al} \dot{\dashv}$   
 $\text{ABSTIME}(\tilde{c}', T)$ , then it must be that, at some point,  
 $\text{REL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} \tilde{i}_T^{al}$ . Since  $\text{REL}(\mathbb{I}'' lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}'' lck))$   
 and  $\text{DL}(\mathbb{I}'' lck) \in \gamma_t(\text{DL}(\tilde{\mathbb{I}}'' lck))$ , it is thus easy to see  
 that  $t_T^{al} \in \gamma_t((\tilde{i}_T^{all} \dot{\dashv} \tilde{i}_T^{al}) \dot{\dashv} \text{DL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv} (\text{REL}(\tilde{\mathbb{I}}'' lck) \dot{\dashv}$   
 $\alpha_t(\{\infty\})))$ .

This concludes the proof. ■

It is important to notice that all the possible orders in which threads can  
 acquire a lock in the concrete case are covered by the abstract transition rela-

tions, even though  $\mathbf{Ti\~{m}e} = \mathbf{Intv}$ . Since  $\mathbf{Ti\~{m}e} = \mathbf{Intv}$ ,  $\mathbf{Thrd}_{exe}$  might differ for concrete and abstract cases as discussed above. This means that even if some thread is the first in a set of threads to issue a lock-statement acting on some lock,  $lck \in \mathbf{Lck}$ , some other thread could issue its corresponding lock  $lck$ -statement first in the abstract case. Lemma 5.55 states that even if this happens, the first thread will be assigned, and eventually acquire,  $lck$  anyway for some transition sequence(s).

**Lemma 5.55 (Properties of owner assignment for lock-transitions):**

*Given the valid concrete configurations (c.f., Definition 4.4), abstract configurations, lock and threads*

$$\begin{aligned}
 c^0 @ \langle [\mathbf{T}, pc_{\mathbf{T}}^0, \mathbb{r}_{\mathbf{T}}^0, t_{\mathbf{T}}^{a^0}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^0, \mathbb{l}^0 \rangle &\in \mathbf{Conf}, \\
 c^i @ \langle [\mathbf{T}, pc_{\mathbf{T}}^i, \mathbb{r}_{\mathbf{T}}^i, t_{\mathbf{T}}^{a^i}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^i, \mathbb{l}^i \rangle &\in \mathbf{Conf}, \\
 c^n @ \langle [\mathbf{T}, pc_{\mathbf{T}}^n, \mathbb{r}_{\mathbf{T}}^n, t_{\mathbf{T}}^{a^n}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^n, \mathbb{l}^n \rangle &\in \mathbf{Conf}, \\
 \tilde{c}^0 @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^0}, \mathbb{r}_{\mathbf{T}}^{\tilde{c}^0}, \tilde{t}_{\mathbf{T}}^{a^0}]_{\mathbf{T} \in \mathbf{Thrd}_{c^0}}, \tilde{\mathbb{x}}^0, \tilde{\mathbb{l}}^0 \rangle &\in \mathbf{C\~{o}nf}, \\
 \tilde{c}^j @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^j}, \mathbb{r}_{\mathbf{T}}^{\tilde{c}^j}, \tilde{t}_{\mathbf{T}}^{a^j}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^j}}, \tilde{\mathbb{x}}^j, \tilde{\mathbb{l}}^j \rangle &\in \mathbf{C\~{o}nf}, \\
 \tilde{c}^k @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^k}, \mathbb{r}_{\mathbf{T}}^{\tilde{c}^k}, \tilde{t}_{\mathbf{T}}^{a^k}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}^k, \tilde{\mathbb{l}}^k \rangle &\in \mathbf{C\~{o}nf}, \\
 lck' &\in \mathbf{Lck}, \\
 \mathbf{T}' &\in \mathbf{Thrd}_{\tilde{c}^k} \text{ and} \\
 \mathbf{T}'' &\in \mathbf{Thrd}_{\tilde{c}^k},
 \end{aligned}$$

such that

$$\begin{aligned}
 & 0 \leq i < n, \\
 & c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^i \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n, \\
 & 0 \leq j < k, \\
 & \tilde{c}^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^j \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^k, \\
 & \mathbf{Thrd}_{\tilde{c}^k} \subseteq \mathbf{Thrd}_{\tilde{c}^j} \subseteq \mathbf{Thrd}_{\tilde{c}^0} \subseteq \mathbf{Thrd}, \\
 & \text{STM}(\mathbf{T}'', pc_{\mathbf{T}''}^n) = [\text{lock } lck']^{pc_{\mathbf{T}''}^n}, \\
 & \mathbf{T}'' \in \mathbf{Thrd}_{exe}^{c^n}, \\
 & \text{STM}(\mathbf{T}', pc_{\mathbf{T}'}^k) = [\text{lock } lck']^{pc_{\mathbf{T}'}^k}, \\
 & \mathbf{T}' \in \mathbf{Thrd}_{exe}^k, \\
 & \forall h \in \{0, \dots, k-1\} : (\mathbf{T}' \in \mathbf{Thrd}_{exe}^h \Rightarrow \text{STM}(\mathbf{T}', pc_{\mathbf{T}'}^h) \neq [\text{lock } lck']^{pc_{\mathbf{T}'}^h}), \\
 & \text{REL}(\mathbb{1}^i lck') \in \gamma_i(\text{REL}(\tilde{\mathbb{1}}^j lck')), \\
 & (pc_{\mathbf{T}'}^i = pc_{\mathbf{T}'}^k \wedge \\
 & \quad t_{\mathbf{T}'}^i \in \gamma_i(\tilde{t}_{\mathbf{T}'}^k) \wedge \\
 & \quad \mathbf{T}' \in \mathbf{Thrd}_{exe}^i \wedge \\
 & \quad \text{OWN}(\mathbb{1}^i lck') = \perp_{\text{thrd}} \wedge \\
 & \quad \text{OWN}(\mathbb{1}^{i+1} lck') = \mathbf{T}') \text{ and} \\
 & (pc_{\mathbf{T}''}^n = pc_{\mathbf{T}''}^j \wedge \\
 & \quad t_{\mathbf{T}''}^n \in \gamma_n(\tilde{t}_{\mathbf{T}''}^j) \wedge \\
 & \quad \mathbf{T}'' \in \mathbf{Thrd}_{exe}^{\text{all}^j} \wedge \\
 & \quad \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^j lck') = \perp_{\text{thrd}} \wedge \\
 & \quad \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^{j+1} lck') = \mathbf{T}'),
 \end{aligned}$$

where the trace for  $\mathbf{T}'$  in  $\tilde{c}^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^k$  is the same as in  $c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^i$ , the trace for  $\mathbf{T}''$  in  $\tilde{c}^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^j$  is the same as in  $c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n$ ,  $\mathbf{Thrd}_{exe}^n$  is as defined in Table 4.3, and  $\mathbf{Thrd}_{exe}^{\text{all}^j}$  and  $\mathbf{Thrd}_{exe}^k$  are as defined in Table 5.6,  $\xrightarrow{\text{prg}}$  satisfies:

$$\begin{aligned}
 & \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^k lck') = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^{j+1} lck') = \text{OWN}(\mathbb{1}^{i+1} lck') = \mathbf{T}' \wedge \\
 & \text{STT}(\mathbb{1}^i lck') = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}}^j lck') = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}}^{j+1} lck') = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}}^k lck') = \text{unlocked} \wedge \\
 & \text{D}\tilde{\text{L}}(\tilde{\mathbb{1}}^k lck') = \text{D}\tilde{\text{L}}(\tilde{\mathbb{1}}^{j+1} lck') \wedge \\
 & \min(\gamma_i(\text{D}\tilde{\text{L}}(\tilde{\mathbb{1}}^k lck'))) = -\infty \wedge \\
 & t_{\mathbf{T}'}^i + \text{TIME}(c^i, \mathbf{T}') \in \gamma_i(\text{D}\tilde{\text{L}}(\tilde{\mathbb{1}}^k lck'))
 \end{aligned}$$

□

PROOF. Assume that the valid concrete configurations, abstract configurations, lock and threads

$$\begin{aligned}
 c^0 @ \langle [\mathbf{T}, pc_{\mathbf{T}}^0, \mathbb{I}_{\mathbf{T}}^0, t_{\mathbf{T}}^{a^0}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{X}^0, \mathbb{I}^0 \rangle &\in \mathbf{Conf}, \\
 c^i @ \langle [\mathbf{T}, pc_{\mathbf{T}}^i, \mathbb{I}_{\mathbf{T}}^i, t_{\mathbf{T}}^{a^i}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{X}^i, \mathbb{I}^i \rangle &\in \mathbf{Conf}, \\
 c^n @ \langle [\mathbf{T}, pc_{\mathbf{T}}^n, \mathbb{I}_{\mathbf{T}}^n, t_{\mathbf{T}}^{a^n}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{X}^n, \mathbb{I}^n \rangle &\in \mathbf{Conf}, \\
 \tilde{c}^0 @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^0}, \tilde{\mathbb{I}}_{\mathbf{T}}^0, \tilde{t}_{\mathbf{T}}^{a^0}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^0}}, \tilde{\mathbb{X}}^0, \tilde{\mathbb{I}}^0 \rangle &\in \mathbf{C\tilde{on}f}, \\
 \tilde{c}^j @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^j}, \tilde{\mathbb{I}}_{\mathbf{T}}^j, \tilde{t}_{\mathbf{T}}^{a^j}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^j}}, \tilde{\mathbb{X}}^j, \tilde{\mathbb{I}}^j \rangle &\in \mathbf{C\tilde{on}f}, \\
 \tilde{c}^k @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^k}, \tilde{\mathbb{I}}_{\mathbf{T}}^k, \tilde{t}_{\mathbf{T}}^{a^k}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{X}}^k, \tilde{\mathbb{I}}^k \rangle &\in \mathbf{C\tilde{on}f}, \\
 lck' &\in \mathbf{Lck}, \\
 \mathbf{T}' &\in \mathbf{Thrd}_{\tilde{c}^k} \text{ and} \\
 \mathbf{T}'' &\in \mathbf{Thrd}_{\tilde{c}^k},
 \end{aligned}$$

are such that

$$\begin{aligned}
 &0 \leq i < n, \\
 &c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^i \xrightarrow{prg} \dots \xrightarrow{prg} c^n, \\
 &0 \leq j < k, \\
 &\tilde{c}^0 \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}^j \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}^k, \\
 &\mathbf{Thrd}_{\tilde{c}^k} \subseteq \mathbf{Thrd}_{\tilde{c}^j} \subseteq \mathbf{Thrd}_{\tilde{c}^0} \subseteq \mathbf{Thrd}, \\
 &\mathbf{STM}(\mathbf{T}'', pc_{\mathbf{T}''}^n) = [\mathbf{lock} \ lck']^{pc_{\mathbf{T}''}^n}, \\
 &\quad \mathbf{T}'' \in \mathbf{Thrd}_{exe}^n, \\
 &\mathbf{STM}(\mathbf{T}', pc_{\mathbf{T}'}^{\tilde{c}^k}) = [\mathbf{lock} \ lck']^{pc_{\mathbf{T}'}^{\tilde{c}^k}}, \\
 &\quad \mathbf{T}' \in \mathbf{Thrd}_{exe}^{\tilde{c}^k}, \\
 &\forall h \in \{0, \dots, k-1\} : (\mathbf{T}' \in \mathbf{Thrd}_{exe}^{\tilde{c}^h} \Rightarrow \mathbf{STM}(\mathbf{T}', pc_{\mathbf{T}'}^{\tilde{c}^h}) \neq [\mathbf{lock} \ lck']^{pc_{\mathbf{T}'}^{\tilde{c}^h}}), \\
 &\quad \mathbf{REL}(\mathbb{I}^i \ lck') \in \gamma_i(\mathbf{REL}(\tilde{\mathbb{I}}^j \ lck')), \\
 &\quad (pc_{\mathbf{T}'}^i = pc_{\mathbf{T}'}^{\tilde{c}^k} \wedge \\
 &\quad t_{\mathbf{T}'}^i \in \gamma_i(\tilde{t}_{\mathbf{T}'}^{\tilde{c}^k}) \wedge \\
 &\quad \mathbf{T}' \in \mathbf{Thrd}_{exe}^i \wedge \\
 &\quad \mathbf{OWN}(\mathbb{I}^i \ lck') = \perp_{thrd} \wedge \\
 &\quad \mathbf{OWN}(\mathbb{I}^{i+1} \ lck') = \mathbf{T}') \text{ and} \\
 &\quad (pc_{\mathbf{T}''}^n = pc_{\mathbf{T}''}^{\tilde{c}^j} \wedge \\
 &\quad t_{\mathbf{T}''}^n \in \gamma_n(\tilde{t}_{\mathbf{T}''}^{\tilde{c}^j}) \wedge \\
 &\quad \mathbf{T}'' \in \mathbf{Thrd}_{exe}^{all^{\tilde{c}^j}} \wedge \\
 &\quad \mathbf{O\tilde{W}N}(\tilde{\mathbb{I}}^j \ lck') = \perp_{thrd} \wedge \\
 &\quad \mathbf{O\tilde{W}N}(\tilde{\mathbb{I}}^{j+1} \ lck') = \mathbf{T}'),
 \end{aligned}$$

where the trace for  $T'$  in  $\tilde{c}^0 \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}^k$  is the same as in  $c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^i$ , the trace for  $T''$  in  $\tilde{c}^0 \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}^j$  is the same as in  $c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^n$ ,  $\mathbf{Thrd}_{exe}^{c^n}$  is as defined in Table 4.3, and  $\mathbf{Thrd}_{exe}^{all\tilde{c}^j}$  and  $\mathbf{Thrd}_{exe}^{\tilde{c}^k}$  are as defined in Table 5.6.

First note that since the trace for  $T'$  in  $\tilde{c}^0 \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}^k$  is the same as in  $c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^i$ , the trace for  $T''$  in  $\tilde{c}^0 \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}^j$  is the same as in  $c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^n$ ,  $\text{STM}(T'', pc_{T''}^n) = [\text{lock } lck']^{pc_{T''}^n}$ ,  $T'' \in \mathbf{Thrd}_{exe}^{c^n}$ ,  $\text{STM}(T', pc_{T'}^{\tilde{c}^k}) = [\text{lock } lck']^{pc_{T'}^{\tilde{c}^k}}$ ,  $T' \in \mathbf{Thrd}_{exe}^{\tilde{c}^k}$ ,  $pc_{T'}^i = pc_{T'}^{\tilde{c}^k}$ ,  $t_{T'}^i \in \gamma_t(\tilde{\tau}_{T'}^k)$ ,  $T' \in \mathbf{Thrd}_{exe}^{c^i}$ ,  $\text{OWN}(\mathbb{I}^i lck') = \perp_{thrd}$ ,  $\text{OWN}(\mathbb{I}^{i+1} lck') = T'$ ,  $pc_{T''}^n = pc_{T''}^{\tilde{c}^j}$ ,  $t_{T''}^n \in \gamma_t(\tilde{\tau}_{T''}^j)$ ,  $\text{OWN}(\mathbb{I}^j lck') = \perp_{thrd}$  and  $\text{OWN}(\mathbb{I}^{j+1} lck') = T''$ , it must be that  $T'$  acquires  $lck'$  in the transition between  $c^i$  and  $c^{i+1}$  and  $T''$  wants to acquire  $lck'$  in a transition from  $c^n$ , while the abstract trace represents a situation (that can occur due to that  $\mathbf{Time} = \mathbf{Intv}$ ) where  $T''$  reaches the  $\text{lock } lck'$ -statement (i.e., it reaches  $pc_{T''}^n$ ) before  $T'$  (i.e., before  $T'$  reaches  $pc_{T'}^i$ ), but  $lck'$  is assigned to  $T'$  as shown below.

Since  $\forall h \in \{0, \dots, k-1\} : (T' \in \mathbf{Thrd}_{exe}^{\tilde{c}^h} \Rightarrow \text{STM}(T', pc_{T'}^{\tilde{c}^h}) \neq [\text{lock } lck']^{pc_{T'}^{\tilde{c}^h}})$ ,  $\text{OWN}(\mathbb{I}^i lck') = \perp_{thrd}$ ,  $\text{OWN}(\mathbb{I}^j lck') = \perp_{thrd}$  and  $\text{OWN}(\mathbb{I}^{j+1} lck') = T''$ , it is easy to see that  $\text{OWN}(\mathbb{I}^k lck') = \text{OWN}(\mathbb{I}^{j+1} lck') = \text{OWN}(\mathbb{I}^{i+1} lck') = T'$ ,  $\text{STT}(\mathbb{I}^i lck') = \text{STT}(\mathbb{I}^j lck') = \text{STT}(\mathbb{I}^{j+1} lck') = \text{STT}(\mathbb{I}^k lck') = \text{unlocked}$  and  $\text{DL}(\mathbb{I}^k lck') = \text{DL}(\mathbb{I}^{j+1} lck')$  (c.f., Table 5.6).

Since  $\text{DLLOCK}$  is used to determine  $\text{DL}(\mathbb{I}^{j+1} lck')$  and  $\text{DL}(\mathbb{I}^k lck') = \text{DL}(\mathbb{I}^{j+1} lck')$ , it is easy to see that  $\min(\gamma_t(\text{DL}(\mathbb{I}^k lck'))) = -\infty$  since  $\text{DLLOCK}$  is used only if  $\exists T \in \mathbf{Thrd}_{exe}^{all\tilde{c}^j} : \text{STM}(T, pc_T^{\tilde{c}^j}) = [\text{lock } lck']^{pc_T^{\tilde{c}^j}}$  (c.f., Table 5.6) which is the case since  $pc_{T''}^n = pc_{T''}^{\tilde{c}^j}$ ,  $\text{OWN}(\mathbb{I}^j lck') = \perp_{thrd}$  and  $\text{OWN}(\mathbb{I}^{j+1} lck') = T''$  (c.f., Algorithm 5.11).

Since  $T' \in \mathbf{Thrd}_{exe}^{c^i}$ , it must be that  $t_{T'}^i + \text{TIME}(c^i, T') = \min(\{t_{T'}^i + \text{TIME}(c^i, T) \mid T \in \mathbf{Thrd}\})$ , and since  $T'' \in \mathbf{Thrd}_{exe}^{c^n}$ , it must be that  $t_{T''}^n + \text{TIME}(c^n, T'') = \min(\{t_{T''}^n + \text{TIME}(c^n, T) \mid T \in \mathbf{Thrd}\})$ . But since  $c^i \xrightarrow{prg} \dots \xrightarrow{prg} c^n$ , it must be that  $t_{T'}^i + \text{TIME}(c^i, T') \leq t_{T''}^n + \text{TIME}(c^n, T'')$  (Lemma 4.2). Note that by choosing  $c^0, c^m, c^n, \tilde{c}^0$  and  $\tilde{c}^j$  (defined by Lemma 5.53) to be  $c^n, c^n, c^n, \tilde{c}^j$  and  $\tilde{c}^j$  (defined by this proof), respectively, and assuming that  $\text{OWN}(\mathbb{I}^n lck') = \perp_{thrd}$  and  $\text{REL}(\mathbb{I}^n lck') \in \gamma_t(\text{REL}(\mathbb{I}^j lck'))$  (which is actually not necessarily the case since  $T'$  acquires  $lck'$  in the transition between  $c^i$  and  $c^{i+1}$ ; however, note that this assumption is okay since if  $T'$  would not

acquire  $lck'$ , then  $\text{OWN}(\mathbb{I}^n lck') = \perp_{\text{thrd}}$  and  $\text{REL}(\mathbb{I}^n lck') \in \gamma_t(\text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^j lck'))$  would hold since  $\text{OWN}(\mathbb{I}^i lck') = \perp_{\text{thrd}}$  and  $\text{REL}(\mathbb{I}^i lck') \in \gamma_t(\text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^j lck'))$ , it is easy to see that  $t_{T''}^{a^n} + \text{TIME}(c^n, T'') \in \gamma_t(\text{DL}\text{LOCK}(\tilde{c}^j, lck'))$  since  $\mathbf{Thrd}_{\tilde{c}^k} \subseteq \mathbf{Thrd}_{\tilde{c}^j} \subseteq \mathbf{Thrd}_{\tilde{c}^0} \subseteq \mathbf{Thrd}$ ,  $\text{STM}(T'', pc_{T''}^n) = [\text{lock } lck']^{pc_{T''}^n}$ ,  $T'' \in \mathbf{Thrd}_{\text{exe}}^{c^n}$  and  $t_{T''}^{a^n} \in \gamma_t(\tilde{t}_{T''}^{a^i})$  (Lemma 5.53). But then, since  $\min(\gamma_t(\text{D}\ddot{\text{L}}(\tilde{\mathbb{I}}^k lck'))) = -\infty$ ,  $\text{D}\ddot{\text{L}}(\tilde{\mathbb{I}}^k lck') = \text{DL}\text{LOCK}(\tilde{c}^j, lck')$  and  $t_{T'}^{a^i} + \text{TIME}(c^i, T') \leq t_{T''}^{a^n} + \text{TIME}(c^n, T'')$ , it must be that  $t_{T'}^{a^i} + \text{TIME}(c^i, T') \in \gamma_t(\text{D}\ddot{\text{L}}(\tilde{\mathbb{I}}^k lck'))$  which concludes the proof. ■

Three lemmas will be presented in order to prove that the abstract transitions described by  $\xrightarrow[\text{prg}]{\sim}$  safely approximate the concrete transitions described by  $\xrightarrow[\text{prg}]{}.$  The lemmas hold given that the concrete transition sequences are finite in length (i.e., given that they terminate) and that either no thread issues a load-statement on a global variable or that the thread issuing the load-statement is the sole thread in  $\mathbf{Thrd}_{\text{exe}}$  in any step of the transition sequence. The first lemma shows that the halt-, skip-, :=-, if-, load-, store- and unlock-statements, and also the lock-statement if the issuing thread immediately is assigned the lock, are safely approximated (Lemma 5.56). Note that a variable is considered global if it could transfer data between two or more threads (c.f., Algorithm 6.9).

**Lemma 5.56 (Soundness of  $\xrightarrow[\text{prg}]{\sim}$ , no frozen thread):**

Given the valid concrete configurations (c.f., Definition 4.4), abstract configurations and thread

$$\begin{aligned} c^0 @ \langle [\mathbb{T}, pc_{\mathbb{T}}^0, \mathbb{x}_{\mathbb{T}}^0, t_{\mathbb{T}}^{a^0}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}^0, \mathbb{I}^0 \rangle &\in \mathbf{Conf}, \\ c^n @ \langle [\mathbb{T}, pc_{\mathbb{T}}^n, \mathbb{x}_{\mathbb{T}}^n, t_{\mathbb{T}}^{a^n}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}^n, \mathbb{I}^n \rangle &\in \mathbf{Conf}, \\ \tilde{c}^0 @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}^0}, \tilde{\mathbb{x}}_{\mathbb{T}}^0, \tilde{t}_{\mathbb{T}}^{a^0}]_{\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}^0}}, \tilde{\mathbb{x}}^0, \tilde{\mathbb{I}}^0 \rangle &\in \mathbf{C\ddot{o}nf}, \\ \tilde{c}^k @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}^k}, \tilde{\mathbb{x}}_{\mathbb{T}}^k, \tilde{t}_{\mathbb{T}}^{a^k}]_{\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}^k, \tilde{\mathbb{I}}^k \rangle &\in \mathbf{C\ddot{o}nf}, \text{ and} \\ T' &\in \mathbf{Thrd}_{\tilde{c}^k}, \end{aligned}$$

such that

$$\begin{aligned}
 & 0 \leq n, \\
 & c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n, \\
 & 0 \leq k, \\
 & \tilde{c}^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^k, \\
 & \mathbf{Thrd}_{\tilde{c}^k} \subseteq \mathbf{Thrd}_{c^0} \subseteq \mathbf{Thrd}, \\
 & pc_{T'}^0 = pc_{T'}^{\tilde{c}^0}, \\
 & \mathbb{I}_{T'}^0 \in \gamma_{\text{reg}}(\tilde{\mathbb{I}}_{T'}^0), \\
 & t_{T'}^a \in \gamma_t(\tilde{t}_{T'}^a), \\
 & \exists \mathbb{x}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}^0) : \forall x \in \mathbf{Var} : \forall T \in \mathbf{Thrd} : ((\mathbb{x}' \ x) \ T) \subseteq ((\mathbb{x}' \ x) \ T), \\
 \forall lck \in \mathbf{Lck} : ((\text{OWN}(\mathbb{I}^0 \ lck) \neq \perp_{\text{thrd}} \Rightarrow & (\text{STT}(\mathbb{I}^0 \ lck) = \text{STT}(\tilde{\mathbb{I}}^0 \ lck) \wedge \\
 & \text{OWN}(\mathbb{I}^0 \ lck) = \text{OWN}(\tilde{\mathbb{I}}^0 \ lck) \wedge \\
 & \text{DL}(\mathbb{I}^0 \ lck) \in \gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 \ lck)) \wedge \\
 & \text{POWN}(\mathbb{I}^0 \ lck) = \text{POWN}(\tilde{\mathbb{I}}^0 \ lck) \wedge \\
 & \text{REL}(\mathbb{I}^0 \ lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}^0 \ lck)) \wedge \\
 & \min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 \ lck))) = -\infty)) \wedge \\
 (\text{OWN}(\mathbb{I}^0 \ lck) = \perp_{\text{thrd}} \Rightarrow & ((\text{OWN}(\mathbb{I}^0 \ lck) = \text{OWN}(\tilde{\mathbb{I}}^0 \ lck) \vee \\
 & (\text{OWN}(\tilde{\mathbb{I}}^0 \ lck) = T' \wedge \\
 & \text{STT}(\tilde{\mathbb{I}}^0 \ lck) = \text{unlocked} \wedge \\
 & t_{T'}^a + \text{TIME}(c^n, T') \in \gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 \ lck)) \wedge \\
 & \min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 \ lck))) = -\infty)) \wedge \\
 & \text{POWN}(\mathbb{I}^0 \ lck) = \text{POWN}(\tilde{\mathbb{I}}^0 \ lck) \wedge \\
 & \text{REL}(\mathbb{I}^0 \ lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}^0 \ lck)) \wedge \\
 & \text{STM}(T', pc_{T'}^0) = [\text{lock } lck]^{pc_{T'}^0} \Rightarrow \\
 & \quad (\mathbb{I}^n \ lck = \mathbb{I}^0 \ lck \wedge \\
 & \quad \tilde{\mathbb{I}}^k \ lck = \tilde{\mathbb{I}}^0 \ lck))), \\
 & \forall i \in \{0, \dots, n-1\} : T' \notin \mathbf{Thrd}_{\text{exe}}^i, \\
 & \text{STM}(T', pc_{T'}^n) \neq [\text{halt}]^{pc_{T'}^n} \Rightarrow T' \in \mathbf{Thrd}_{\text{exe}}^n, \\
 & \forall i \in \{0, \dots, k-1\} : T' \notin \mathbf{Thrd}_{\text{exe}}^i, \\
 & \text{STM}(T', pc_{T'}^k) \neq [\text{halt}]^{pc_{T'}^k} \Rightarrow T' \in \mathbf{Thrd}_{\text{exe}}^k, \text{ and} \\
 \forall i \in \{0, \dots, k\} : (|\mathbf{Thrd}_{\text{exe}}^i| \neq 1 \vee & \\
 \{T \in \mathbf{Thrd}_{\text{exe}}^i \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : & \\
 \text{STM}(T, pc_T^i) = [\text{load } r \text{ from } x]^{pc_T^i} = \emptyset), &
 \end{aligned}$$

where for all  $i \in \{0, \dots, n\}$ ,  $\mathbf{Thrd}_{\text{exe}}^i$  is as defined in Table 4.3, for all  $i \in \{0, \dots, k\}$ ,  $\mathbf{Thrd}_{\text{exe}}^i$  is as defined in Table 5.6, and  $\mathbf{Var}_g$  contains all  $x \in \mathbf{Var}$

such that  $x$  can be written to by one thread and read from by another thread (i.e., there might be a data dependency between the threads; note that  $\mathbf{Var}_g$  can be derived using Algorithm 6.9),  $\xrightarrow{prg}$  satisfies:

$$\begin{aligned}
 & \forall c @ \langle [\mathbb{T}, pc_{\mathbb{T}}, \mathbb{r}_{\mathbb{T}}, t_{\mathbb{T}}^a]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf} : \\
 & (c^n \xrightarrow{prg} c \Rightarrow \exists \tilde{c} @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}}, \tilde{\mathbb{r}}_{\mathbb{T}}, \tilde{t}_{\mathbb{T}}^a]_{\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \mathbf{C\tilde{on}f} : \\
 & \quad (\tilde{c}^k \xrightarrow{prg} \tilde{c} \wedge \\
 & \quad pc_{\mathbb{T}'} = pc_{\mathbb{T}'}^{\tilde{c}} \wedge \\
 & \quad \mathbb{r}_{\mathbb{T}'} \in \gamma_{reg}(\tilde{\mathbb{r}}_{\mathbb{T}'}) \wedge \\
 & \quad t_{\mathbb{T}'}^a \in \gamma_t(\tilde{t}_{\mathbb{T}'}^a) \wedge \\
 & \quad \exists \mathbb{x}' \in \gamma_{var}(\tilde{\mathbb{x}}) : (\forall x \in \mathbf{Var} : ((\mathbb{x} \ x) \mathbb{T}') \subseteq ((\mathbb{x}' \ x) \mathbb{T}')) \wedge \\
 & \quad \forall lck \in \mathbf{Lck} : ((\mathbf{OWN}(\mathbb{l}^0 \ lck) = \mathbb{T}' \vee \mathbf{OWN}(\mathbb{l} \ lck) = \mathbb{T}') \Rightarrow \\
 & \quad \quad (\mathbf{STT}(\mathbb{l} \ lck) = \mathbf{STT}(\tilde{\mathbb{l}} \ lck) \wedge \\
 & \quad \quad \mathbf{OWN}(\mathbb{l} \ lck) = \mathbf{OWN}(\tilde{\mathbb{l}} \ lck) \wedge \\
 & \quad \quad \mathbf{DL}(\mathbb{l} \ lck) \in \gamma_t(\mathbf{DL}(\tilde{\mathbb{l}} \ lck)) \wedge \\
 & \quad \quad \mathbf{POWN}(\mathbb{l} \ lck) = \mathbf{POWN}(\tilde{\mathbb{l}} \ lck) \wedge \\
 & \quad \quad \mathbf{REL}(\mathbb{l} \ lck) \in \gamma_t(\mathbf{REL}(\tilde{\mathbb{l}} \ lck)) \wedge \\
 & \quad \quad \min(\gamma_t(\mathbf{DL}(\tilde{\mathbb{l}} \ lck))) = -\infty))) \quad \square
 \end{aligned}$$

PROOF. Assume that the valid concrete configurations (c.f., Definition 4.4), abstract configurations and thread

$$\begin{aligned}
 & c^0 @ \langle [\mathbb{T}, pc_{\mathbb{T}}^0, \mathbb{r}_{\mathbb{T}}^0, t_{\mathbb{T}}^{a^0}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}^0, \mathbb{l}^0 \rangle \in \mathbf{Conf}, \\
 & c^n @ \langle [\mathbb{T}, pc_{\mathbb{T}}^n, \mathbb{r}_{\mathbb{T}}^n, t_{\mathbb{T}}^{a^n}]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}^n, \mathbb{l}^n \rangle \in \mathbf{Conf}, \\
 & \tilde{c}^0 @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}^0}, \tilde{\mathbb{r}}_{\mathbb{T}}^0, \tilde{t}_{\mathbb{T}}^{a^0}]_{\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}^0}}, \tilde{\mathbb{x}}^0, \tilde{\mathbb{l}}^0 \rangle \in \mathbf{C\tilde{on}f}, \\
 & \tilde{c}^k @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}^k}, \tilde{\mathbb{r}}_{\mathbb{T}}^k, \tilde{t}_{\mathbb{T}}^{a^k}]_{\mathbb{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}^k, \tilde{\mathbb{l}}^k \rangle \in \mathbf{C\tilde{on}f}, \text{ and} \\
 & \mathbb{T}' \in \mathbf{Thrd}_{\tilde{c}^k},
 \end{aligned}$$



are such that

$$\begin{aligned}
 & 0 \leq n, \\
 & c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^n, \\
 & 0 \leq k, \\
 & \tilde{c}^0 \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}^k, \\
 & \mathbf{Thrd}_{\tilde{c}^k} \subseteq \mathbf{Thrd}_{c^0} \subseteq \mathbf{Thrd}, \\
 & pc_{T'}^0 = pc_{T'}^{\tilde{c}^0}, \\
 & \mathbb{I}_{T'}^0 \in \gamma_{reg}(\tilde{\mathbb{I}}_{T'}^0), \\
 & t_{T'}^a \in \gamma_t(\tilde{t}_{T'}^a), \\
 & \exists \mathbb{x}' \in \gamma_{var}(\tilde{\mathbb{x}}^0) : \forall x \in \mathbf{Var} : \forall T \in \mathbf{Thrd} : ((\mathbb{x}' x) T) \subseteq ((\mathbb{x}' x) T), \\
 & \forall lck \in \mathbf{Lck} : ((\mathbf{OWN}(\mathbb{I}^0 lck) \neq \perp_{thrd} \Rightarrow (\mathbf{STT}(\mathbb{I}^0 lck) = \mathbf{S\tilde{T}T}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \mathbf{OWN}(\mathbb{I}^0 lck) = \mathbf{O\tilde{W}N}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \mathbf{DL}(\mathbb{I}^0 lck) \in \gamma_t(\mathbf{D\tilde{L}}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \mathbf{POWN}(\mathbb{I}^0 lck) = \mathbf{PO\tilde{W}N}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \mathbf{REL}(\mathbb{I}^0 lck) \in \gamma_t(\mathbf{R\tilde{E}L}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \min(\gamma_t(\mathbf{D\tilde{L}}(\tilde{\mathbb{I}}^0 lck))) = -\infty)) \wedge \\
 & (\mathbf{OWN}(\mathbb{I}^0 lck) = \perp_{thrd} \Rightarrow ((\mathbf{OWN}(\mathbb{I}^0 lck) = \mathbf{O\tilde{W}N}(\tilde{\mathbb{I}}^0 lck) \vee \\
 & \quad (\mathbf{O\tilde{W}N}(\tilde{\mathbb{I}}^0 lck) = T' \wedge \\
 & \quad \mathbf{S\tilde{T}T}(\tilde{\mathbb{I}}^0 lck) = \mathbf{unlocked} \wedge \\
 & \quad t_{T'}^a + \mathbf{TIME}(c^n, T') \in \gamma_t(\mathbf{D\tilde{L}}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \min(\gamma_t(\mathbf{D\tilde{L}}(\tilde{\mathbb{I}}^0 lck))) = -\infty)) \wedge \\
 & \quad \mathbf{POWN}(\mathbb{I}^0 lck) = \mathbf{PO\tilde{W}N}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \mathbf{REL}(\mathbb{I}^0 lck) \in \gamma_t(\mathbf{R\tilde{E}L}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \mathbf{STM}(T', pc_{T'}^0) = [\mathbf{lock} lck]^{pc_{T'}^0} \Rightarrow \\
 & \quad (\mathbb{I}^n lck = \mathbb{I}^0 lck \wedge \\
 & \quad \tilde{\mathbb{I}}^k lck = \tilde{\mathbb{I}}^0 lck))), \\
 & \forall i \in \{0, \dots, n-1\} : T' \notin \mathbf{Thrd}_{exe}^i, \\
 & \mathbf{STM}(T', pc_{T'}^n) \neq [\mathbf{halt}]^{pc_{T'}^n} \Rightarrow T' \in \mathbf{Thrd}_{exe}^n, \\
 & \forall i \in \{0, \dots, k-1\} : T' \notin \mathbf{Thrd}_{exe}^i, \\
 & \mathbf{STM}(T', pc_{T'}^k) \neq [\mathbf{halt}]^{pc_{T'}^k} \Rightarrow T' \in \mathbf{Thrd}_{exe}^k, \text{ and} \\
 & \forall i \in \{0, \dots, k\} : (|\mathbf{Thrd}_{exe}^i| \neq 1 \vee \\
 & \quad \{T \in \mathbf{Thrd}_{exe}^i \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : \\
 & \quad \quad \mathbf{STM}(T, pc_T^i) = [\mathbf{load} r \text{ from } x]^{pc_T^i} = \emptyset\}),
 \end{aligned}$$

where for all  $i \in \{0, \dots, n\}$ ,  $\mathbf{Thrd}_{exe}^i$  is as defined in Table 4.3, for all  $i \in \{0, \dots, k\}$ ,  $\mathbf{Thrd}_{exe}^i$  is as defined in Table 5.6, and  $\mathbf{Var}_g$  contains all  $x \in \mathbf{Var}$

such that  $x$  can be written to by one thread and read from by another thread (i.e., there might be a data dependency between the threads).

First note that:

- Since  $\forall i \in \{0, \dots, n-1\} : T' \notin \mathbf{Thrd}_{exe}^{c^i}$ , it must be that  $pc_{T'}^n = pc_{T'}^0$ ,  $\mathbb{r}_{T'}^n = \mathbb{r}_{T'}^0$ ,  $t_{T'}^n = t_{T'}^0$  and  $\forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{l}^0 lck) = T' \Rightarrow \mathbb{l}^n lck = \mathbb{l}^0 lck)$  (c.f., Table 4.3).
- Since  $\forall i \in \{0, \dots, k-1\} : T' \notin \mathbf{Thrd}_{exe}^{c^i}$ , it must be that  $pc_{T'}^k = pc_{T'}^0$ ,  $\tilde{\mathbb{r}}_{T'}^k = \tilde{\mathbb{r}}_{T'}^0$ ,  $\tilde{t}_{T'}^k = \tilde{t}_{T'}^0$  and  $\forall lck \in \mathbf{Lck} : (\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^0 lck) = T' \Rightarrow (\tilde{\mathbb{l}}^k lck = \tilde{\mathbb{l}}^0 lck \wedge \min(\gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{l}}^k lck))) = -\infty))$ .
- Since  $pc_{T'}^n = pc_{T'}^0$ ,  $\mathbb{r}_{T'}^n = \mathbb{r}_{T'}^0$ ,  $t_{T'}^n = t_{T'}^0$ ,  $\forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{l}^0 lck) = T' \Rightarrow \mathbb{l}^n lck = \mathbb{l}^0 lck)$ ,  $pc_{T'}^k = pc_{T'}^0$ ,  $\tilde{\mathbb{r}}_{T'}^k = \tilde{\mathbb{r}}_{T'}^0$ ,  $\tilde{t}_{T'}^k = \tilde{t}_{T'}^0$ ,  $\forall lck \in \mathbf{Lck} : (\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^0 lck) = T' \Rightarrow (\tilde{\mathbb{l}}^k lck = \tilde{\mathbb{l}}^0 lck \wedge \min(\gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{l}}^k lck))) = -\infty))$ ,  $pc_{T'}^0 = pc_{T'}^0$ ,  $\mathbb{r}_{T'}^0 \in \gamma_{reg}(\tilde{\mathbb{r}}_{T'}^0)$ ,  $t_{T'}^0 \in \gamma_t(\tilde{t}_{T'}^0)$  and  $\forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{l}^0 lck) = T' \Rightarrow (\text{STT}(\mathbb{l}^0 lck) = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{l}}^0 lck) \wedge \text{OWN}(\mathbb{l}^0 lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^0 lck) \wedge \text{DL}(\mathbb{l}^0 lck) \in \gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{l}}^0 lck)) \wedge \text{POW}\text{N}(\mathbb{l}^0 lck) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^0 lck) \wedge \text{REL}(\mathbb{l}^0 lck) \in \gamma_t(\tilde{\text{R}}\tilde{\text{E}}\text{L}(\tilde{\mathbb{l}}^0 lck)) \wedge \min(\gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{l}}^0 lck))) = -\infty))$ , it must be that:

$$\begin{aligned}
 pc_{T'}^n &= pc_{T'}^k \wedge \\
 \mathbb{r}_{T'}^n &\in \gamma_{reg}(\tilde{\mathbb{r}}_{T'}^k) \wedge \\
 t_{T'}^n &\in \gamma_t(\tilde{t}_{T'}^k) \wedge \\
 \forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{l}^n lck) = T' \Rightarrow &(\text{STT}(\mathbb{l}^n lck) = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{l}}^k lck) \wedge \\
 &\text{OWN}(\mathbb{l}^n lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^k lck) \wedge \\
 &\text{DL}(\mathbb{l}^n lck) \in \gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{l}}^k lck)) \wedge \\
 &\text{POW}\text{N}(\mathbb{l}^n lck) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^k lck) \wedge \\
 &\text{REL}(\mathbb{l}^n lck) \in \gamma_t(\tilde{\text{R}}\tilde{\text{E}}\text{L}(\tilde{\mathbb{l}}^k lck)) \wedge \\
 &\min(\gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{l}}^k lck))) = -\infty))
 \end{aligned}$$

- Since  $c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^n$  and  $\forall i \in \{0, \dots, n-1\} : T' \notin \mathbf{Thrd}_{exe}^{c^i}$ , it must be that for all  $x \in \mathbf{Var}$ ,  $((\mathbb{x}^n x) T') = ((\mathbb{x}^0 x) T')$  if no thread writes to  $x$  in the sequence  $c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^n$ , or  $((\mathbb{x}^n x) T') = \emptyset$  if some other thread has written to  $x$  in the given sequence (c.f., Table 4.3). Thus,  $\forall x \in \mathbf{Var} : ((\mathbb{x}^n x) T') \subseteq ((\mathbb{x}^0 x) T')$ .

- Since  $\exists \mathbb{X}' \in \gamma_{var}(\tilde{\mathbb{X}}^0) : \forall x \in \mathbf{Var} : ((\mathbb{X}^0 x) T') \subseteq ((\mathbb{X}' x) T')$ ,  $c^0 \xrightarrow{prg} \dots \xrightarrow{prg} c^n$ ,  $\tilde{c}^0 \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}^k$ ,  $\forall i \in \{0, \dots, n-1\} : T' \notin \mathbf{Thrd}_{exe}^{ci}$ ,  $\forall i \in \{0, \dots, k-1\} : T' \notin \mathbf{Thrd}_{exe}^{ci}$  and TRIM is safe (Lemma 5.27), it must be that  $\exists \mathbb{X}' \in \gamma_{var}(\tilde{\mathbb{X}}^k) : \forall x \in \mathbf{Var} : ((\mathbb{X}^n x) T') \subseteq ((\mathbb{X}' x) T')$ .
- Since  $\forall i \in \{0, \dots, k\} : (|\mathbf{Thrd}_{exe}^{ci}| \not\approx 1 \vee \{T \in \mathbf{Thrd}_{exe}^{ci} \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : \text{STM}(T, pc_T^{ci}) = [\text{load } r \text{ from } x]^{pc_T^{ci}}\} = \emptyset)$ , it must be that  $\forall i \in \{0, \dots, k\} : (\{T \in \mathbf{Thrd}_{exe}^{ci} \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : \text{STM}(T, pc_T^{ci}) = [\text{load } r \text{ from } x]^{pc_T^{ci}}\} \neq \emptyset \Rightarrow |\mathbf{Thrd}_{exe}^{ci}| = 1)$ . This means that if some thread in  $\mathbf{Thrd}_{exe}^{ci}$ , where  $i \in \{0, \dots, k\}$ , performs a load-statement, there is only one single thread in  $\mathbf{Thrd}_{exe}^{ci}$ ; thus that thread performs the load-statement. It is then easy to see, from the definition of  $\mathbf{Thrd}_{exe}^{ci}$ , that there cannot occur any other write than those represented by  $\tilde{\mathbb{X}}^i$  such that it could affect the load-statement of the thread in  $\mathbf{Thrd}_{exe}^{ci}$  (c.f., Assumption 5.50) – thus, it must be that  $\tilde{\mathbb{X}}^k$  (and also all  $\tilde{\mathbb{X}}^i$ , where  $i \in \{0, \dots, k\}$ ) contains safe write history (c.f., Definition 5.18).
- Since, trivially,  $\forall lck \in \mathbf{Lck} : \{T \in \mathbf{Thrd}_{exe}^{cn} \cap \mathbf{Thrd}_{\check{c}k} \mid \text{STM}(T, pc_T^{cn}) = [\text{lock } lck]^{pc_T^{cn}}\} \subseteq \{T \in \mathbf{Thrd}_{\check{c}k} \mid \exists l \in \mathbf{Lbl}_T : \text{STM}(T, l) = [\text{lock } lck]^l\}$ , it must be that if  $T'$  can be assigned a lock in the concrete case, it can also be assigned the lock in the corresponding abstract case.
- If, for some  $lck \in \mathbf{Lck}$ ,  $\text{STM}(T', pc_{T'}^{\check{c}k}) = [\text{lock } lck]^{pc_{T'}^{\check{c}k}}$ , it must be that  $\text{O}\check{\text{W}}\text{N}(\tilde{\mathbb{I}}^{k''} lck) = T'$ , since  $\forall i \in \{0, \dots, k-1\} : T' \notin \mathbf{Thrd}_{exe}^{ci}$  and  $T' \in \mathbf{Thrd}_{exe}^{\check{c}k}$ .
- Since  $T' \in \mathbf{Thrd}_{\check{c}k}$ ,  $\mathbf{Thrd}_{\check{c}k} \subseteq \mathbf{Thrd}$ ,  $pc_{T'}^{\check{c}k} = pc_{T'}^n$ ,  $t_{T'}^a \in \gamma_t(\tilde{\mathbb{I}}_T^a)$ ,  $\forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{I}^0 lck) = T' \Rightarrow (\text{STT}(\mathbb{I}^n lck) = \text{STT}(\tilde{\mathbb{I}}^k lck) \wedge \text{OWN}(\mathbb{I}^n lck) = \text{O}\check{\text{W}}\text{N}(\tilde{\mathbb{I}}^k lck) \wedge \text{DL}(\mathbb{I}^n lck) \in \gamma_t(\check{\text{D}}\check{\text{L}}(\tilde{\mathbb{I}}^k lck)) \wedge \text{PO}\check{\text{W}}\text{N}(\mathbb{I}^n lck) = \text{PO}\check{\text{W}}\text{N}(\tilde{\mathbb{I}}^k lck) \wedge \text{REL}(\mathbb{I}^n lck) \in \gamma_t(\check{\text{R}}\check{\text{E}}\check{\text{L}}(\tilde{\mathbb{I}}^k lck))))$ ,  $T' \in \mathbf{Thrd}_{exe}^{\check{c}k}$ ,  $T' \in \mathbf{Thrd}_{exe}^{cn}$ ,  $\forall lck \in \mathbf{Lck} : (\text{STM}(T', pc_{T'}^{\check{c}k}) = [\text{lock } lck]^{pc_{T'}^{\check{c}k}} \Rightarrow \text{O}\check{\text{W}}\text{N}(\tilde{\mathbb{I}}^{k''} lck) = T')$ , it must be that  $t_{T'}^a \in \gamma_t(\text{ACCTIME}(\langle [T, pc_T^{\check{c}k}, \tilde{\mathbb{I}}_T^k, \tilde{\mathbb{I}}_T^a]_{T \in \mathbf{Thrd}_{\check{c}k}}, \tilde{\mathbb{X}}^k, \tilde{\mathbb{I}}^{k''} \rangle, \mathbf{Thrd}_{exe}^{\check{c}k}, T'))$  whenever  $\forall lck \in \mathbf{Lck} : (\text{STM}(T', pc_{T'}^n) = [\text{lock } lck]^{pc_{T'}^n} \Rightarrow (\text{O}\check{\text{W}}\text{N}(\tilde{\mathbb{I}}^{k''} lck) = T' \wedge \text{OWN}(\mathbb{I}^{n''} lck) = T'))$  (Lemma 5.54), where  $t_{T'}^a$

is derived from  $c^n \xrightarrow{\text{prg}} \langle [\mathbb{T}, pc_{\mathbb{T}}, \mathbb{T}_{\mathbb{T}}, t_{\mathbb{T}}^a]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle$  and  $\mathbb{I}^{n''}$  and  $\tilde{\mathbb{I}}^{k''}$  are defined as in Tables 4.3 and 5.6, respectively.

- Since  $\forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{I}^0 lck) = \perp_{\text{thrd}} \Rightarrow (\text{STM}(\mathbb{T}', pc_{\mathbb{T}'}^0) = [\text{lock } lck]^{pc_{\mathbb{T}'}} \Rightarrow (\mathbb{I}^n lck = \mathbb{I}^0 lck \wedge \tilde{\mathbb{I}}^k lck = \tilde{\mathbb{I}}^0 lck))), \forall i \in \{0, \dots, n-1\} : \mathbb{T}' \notin \mathbf{Thrd}_{exe}^i, \text{STM}(\mathbb{T}', pc_{\mathbb{T}'}^n) \neq [\text{halt}]^{pc_{\mathbb{T}'}} \Rightarrow \mathbb{T}' \in \mathbf{Thrd}_{exe}^n$  and  $\text{OWN}(\tilde{\mathbb{I}}^{k''} lck) = \mathbb{T}'$ , it must be that  $\mathbb{T}'$  immediately acquires  $lck$  (i.e., without any other thread acquiring and possibly releasing  $lck$  in the sequence  $c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n$ ) if  $\text{STM}(\mathbb{T}', pc_{\mathbb{T}'}^k) = [\text{lock } lck]^{pc_{\mathbb{T}'}}$ , both in the concrete and abstract cases (based on  $c^n$  and  $\tilde{c}^k$ ).
- If, for some lock,  $lck' \in \mathbf{Lck}$ ,  $\text{STM}(\mathbb{T}', pc_{\mathbb{T}'}^0) = [\text{lock } lck']^{pc_{\mathbb{T}'}}$  and  $\text{OWN}(\mathbb{I}^0 lck') = \perp_{\text{thrd}}$ , it must be that  $\min(\{t_{\mathbb{T}'}^a + \text{TIME}(c^n, \mathbb{T}) \mid \mathbb{T} \in \mathbf{Thrd}\}) \in \gamma_t(\text{DLLOCK}(\tilde{c}^j, lck'))$ , since  $\mathbb{T}' \in \mathbf{Thrd}_{ck}^k, \mathbf{Thrd}_{ck}^k \subseteq \mathbf{Thrd}_{c^0} \subseteq \mathbf{Thrd}$ ,  $m, n$  and  $j$  (c.f., Lemma 5.53) can be chosen to be 0,  $n$  and  $k$  (given by this proof), respectively,  $t_{\mathbb{T}'}^a \in \gamma_t(\tilde{t}_{\mathbb{T}'}^a)$ ,  $t_{\mathbb{T}'}^n = t_{\mathbb{T}'}^0, \tilde{t}_{\mathbb{T}'}^k = \tilde{t}_{\mathbb{T}'}^0, pc_{\mathbb{T}'}^k = pc_{\mathbb{T}'}^0 = pc_{\mathbb{T}'}^n = pc_{\mathbb{T}'}^0, \mathbb{T}' \in \mathbf{Thrd}_{exe}^n$  and (since  $\forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{I}^0 lck) = \perp_{\text{thrd}} \Rightarrow (\text{STM}(\mathbb{T}', pc_{\mathbb{T}'}^0) = [\text{lock } lck]^{pc_{\mathbb{T}'}} \Rightarrow (\mathbb{I}^n lck = \mathbb{I}^0 lck \wedge \tilde{\mathbb{I}}^k lck = \tilde{\mathbb{I}}^0 lck)))$  and  $\text{REL}(\mathbb{I}^0 lck') \in \gamma_t(\text{R}\tilde{\text{EL}}(\tilde{\mathbb{I}}^0 lck'))$ )  $\text{REL}(\mathbb{I}^0 lck') \in \gamma_t(\text{R}\tilde{\text{EL}}(\tilde{\mathbb{I}}^k lck'))$  (Lemma 5.53). Thus,  $t_{\mathbb{T}'}^n + \text{TIME}(c^n, \mathbb{T}') \in \gamma_t(\text{DLLOCK}(\tilde{c}^k, lck'))$ , since  $\mathbb{T}' \in \mathbf{Thrd}_{exe}^n$  which means that  $t_{\mathbb{T}'}^n + \text{TIME}(c^n, \mathbb{T}') = \min(\{t_{\mathbb{T}'}^a + \text{TIME}(c^n, \mathbb{T}) \mid \mathbb{T} \in \mathbf{Thrd}\})$  (c.f., Table 4.3).

The proof will now be conducted by considering the different statements that  $\mathbb{T}'$  could issue in  $c^0$  (i.e., in  $c^n$ ).

1. If  $\text{STM}(\mathbb{T}', pc_{\mathbb{T}'}^0) = [\text{halt}]^{pc_{\mathbb{T}'}}$ , then it must be that  $\mathbb{T}' \notin \mathbf{Thrd}_{exe}^n$ . Thus, it must be that  $c^n \xrightarrow{\text{prg}} c$ , where  $c @ \langle [\mathbb{T}, pc_{\mathbb{T}}, \mathbb{T}_{\mathbb{T}}, t_{\mathbb{T}}^a]_{\mathbb{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle$  is such that  $pc_{\mathbb{T}'} = pc_{\mathbb{T}}^n, \mathbb{T}_{\mathbb{T}'} = \mathbb{T}_{\mathbb{T}}^n, t_{\mathbb{T}'}^a = t_{\mathbb{T}}^n, \forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{I}^0 lck) = \mathbb{T}' \Rightarrow \mathbb{I}^n lck = \mathbb{I}^0 lck)$  and  $\forall x \in \mathbf{Var} : ((\mathbb{x} x) \mathbb{T}') \subseteq ((\mathbb{x}^n x) \mathbb{T}')$ , provided that  $\exists \mathbb{T} \in \mathbf{Thrd} : \text{STM}(\mathbb{T}, pc_{\mathbb{T}}^0) \neq [\text{halt}]^{pc_{\mathbb{T}}^0}$  (otherwise  $\xrightarrow{\text{prg}}$  is not applicable; c.f., Table 4.3).

Note that  $\mathbb{T}' \notin \mathbf{Thrd}_{exe}^k$  and choose  $\tilde{c} @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}}, \mathbb{T}_{\mathbb{T}}, \tilde{t}_{\mathbb{T}}^a]_{\mathbb{T} \in \mathbf{Thrd}_{ck}^k}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle$

such that  $\tilde{c}^k \xrightarrow{\text{prg}} \tilde{c}$ , i.e.,  $pc_{\mathbb{T}'}^{\tilde{c}} = pc_{\mathbb{T}'}^k, \mathbb{T}_{\mathbb{T}'} = \mathbb{T}_{\mathbb{T}}^k, \tilde{t}_{\mathbb{T}'}^a = \tilde{t}_{\mathbb{T}}^k, \forall lck \in \mathbf{Lck} :$

$(\text{OWN}(\mathbb{1}^0 lck) = T' \Rightarrow (\tilde{\mathbb{1}} lck = \tilde{\mathbb{1}}^k lck \wedge \min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{1}} lck))) = -\infty))$ .  
 Note that  $\tilde{\mathbb{x}}$  must still be such that for all  $x \in \mathbf{Var}$ ,  $((\tilde{\mathbb{x}} x) T')$  is a safe approximation of the writes performed on  $x$  by  $T'$  since TRIM is safe (Lemma 5.27). Thus, it must be that:

$$\begin{aligned}
 pc_{T'} &= pc_{T'}^{\tilde{c}} \wedge \\
 \mathbb{F}_{T'} &\in \gamma_{\text{reg}}(\tilde{\mathbb{F}}_{T'}) \wedge \\
 t_{T'}^a &\in \gamma_t(\tilde{t}_{T'}^a) \wedge \\
 \exists \tilde{\mathbb{x}}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}) : &(\forall x \in \mathbf{Var} : ((\tilde{\mathbb{x}} x) T') \subseteq ((\tilde{\mathbb{x}}' x) T')) \wedge \\
 \forall lck \in \mathbf{Lck} : &((\text{OWN}(\mathbb{1}^0 lck) = T' \vee \text{OWN}(\mathbb{1} lck) = T') \Rightarrow \\
 &(\text{STT}(\mathbb{1} lck) = \text{s}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}} lck) \wedge \\
 &\text{OWN}(\mathbb{1} lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck) \wedge \\
 &\text{DL}(\mathbb{1} lck) \in \gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{1}} lck)) \wedge \\
 &\text{POWN}(\mathbb{1} lck) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck) \wedge \\
 &\text{REL}(\mathbb{1} lck) \in \gamma_t(\tilde{\text{REL}}(\tilde{\mathbb{1}} lck)) \wedge \\
 &\min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{1}} lck))) = -\infty))
 \end{aligned}$$

2. If, for some  $a \in \mathbf{Aexp}$ ,  $b \in \mathbf{Bexp}$ ,  $l \in \mathbf{Lbl}_{T'}$ ,  $r \in \mathbf{Reg}_{T'}$ ,  $x \in \mathbf{Var}$  and  $lck \in \mathbf{Lck}$ ,  $\text{STM}(T', pc_{T'}^0) \in \{\text{[skip]}^{pc_{T'}^0}, [r := a]^{pc_{T'}^0}, [\text{if } b \text{ goto } l]^{pc_{T'}^0}, [\text{store } r \text{ to } x]^{pc_{T'}^0}, [\text{unlock } lck]^{pc_{T'}^0}\}$ , then let the configuration  $c @ \langle [T, pc_T, \mathbb{F}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{1} \rangle$  be such that  $c \xrightarrow{\text{prg}} c$  and choose  $\tilde{c} @ \langle [T, pc_T^{\tilde{c}}, \tilde{\mathbb{F}}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{\mathbb{x}}, \tilde{\mathbb{1}} \rangle$  such that  $\tilde{c} \xrightarrow{\text{prg}} \tilde{c}$ . Thus, since  $\forall i \in \{0, \dots, n-1\} : T' \notin \mathbf{Thrd}_{\text{exe}}^{c^i}$ ,  $T' \in \mathbf{Thrd}_{\text{exe}}^{c^n}$ ,  $\forall i \in \{0, \dots, k-1\} : T' \notin \mathbf{Thrd}_{\text{exe}}^{\tilde{c}^i}$ ,  $T' \in \mathbf{Thrd}_{\text{exe}}^{\tilde{c}^k}$ ,  $\xrightarrow{\text{ax}}$  is a safe approximation of  $\xrightarrow{\text{ax}}$  (Lemma 5.49), TRIM is safe (Lemma 5.27),  $\mathbf{Thrd}_{\tilde{c}^k} \subseteq \mathbf{Thrd}$  and ACCTIME is safe (Lemma 5.54), it must be that:

$$\begin{aligned}
 pc_{T'} &= pc_{T'}^{\tilde{c}} \wedge \\
 \mathbb{F}_{T'} &\in \gamma_{\text{reg}}(\tilde{\mathbb{F}}_{T'}) \wedge \\
 t_{T'}^a &\in \gamma_t(\tilde{t}_{T'}^a) \wedge \\
 \exists \tilde{\mathbb{x}}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}) : &(\forall x \in \mathbf{Var} : ((\tilde{\mathbb{x}} x) T') \subseteq ((\tilde{\mathbb{x}}' x) T')) \wedge \\
 \forall lck \in \mathbf{Lck} : &((\text{OWN}(\mathbb{1}^0 lck) = T' \vee \text{OWN}(\mathbb{1} lck) = T') \Rightarrow \\
 &(\text{STT}(\mathbb{1} lck) = \text{s}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}} lck) \wedge \\
 &\text{OWN}(\mathbb{1} lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck) \wedge \\
 &\text{DL}(\mathbb{1} lck) \in \gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{1}} lck)) \wedge \\
 &\text{POWN}(\mathbb{1} lck) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck) \wedge \\
 &\text{REL}(\mathbb{1} lck) \in \gamma_t(\tilde{\text{REL}}(\tilde{\mathbb{1}} lck)) \wedge \\
 &\min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{1}} lck))) = -\infty))
 \end{aligned}$$

Note that in the case  $\text{STM}(\mathsf{T}', pc_{\mathsf{T}'}^0) = [\text{if } b \text{ goto } l]^{\text{pc}_{\mathsf{T}'}}_0$ ,  $\tilde{c}$  can be chosen so that the corresponding branch to that taken in  $c$  is taken since  $\mathbb{r}_{\mathsf{T}'}^0 \in \gamma_{\text{reg}}(\tilde{\mathbb{r}}_{\mathsf{T}'}^0)$  (c.f., Table 5.5 and Definition 5.7).

3. If, for some  $r \in \mathbf{Reg}_{\mathsf{T}'}$  and  $x \in \mathbf{Var}$ ,  $\text{STM}(\mathsf{T}', pc_{\mathsf{T}'}^0) = [\text{load } r \text{ from } x]^{\text{pc}_{\mathsf{T}'}}_0$ , then let  $c @ \langle [\mathsf{T}, pc_{\mathsf{T}}, \mathbb{r}_{\mathsf{T}}, t_{\mathsf{T}}^a]_{\mathsf{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle$  be such that  $c^n \xrightarrow{\text{prg}} c$  and choose  $\tilde{c} @ \langle [\mathsf{T}, pc_{\mathsf{T}}^{\tilde{c}}, \tilde{\mathbb{r}}_{\mathsf{T}}, \tilde{t}_{\mathsf{T}}^a]_{\mathsf{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle$  such that  $\tilde{c}^k \xrightarrow{\text{prg}} \tilde{c}$ . Since  $\forall i \in \{0, \dots, n-1\} : \mathsf{T}' \notin \mathbf{Thrd}_{\text{exe}}^i$ ,  $\mathsf{T}' \in \mathbf{Thrd}_{\text{exe}}^n$ ,  $\forall i \in \{0, \dots, k-1\} : \mathsf{T}' \notin \mathbf{Thrd}_{\text{exe}}^i$ ,  $\mathsf{T}' \in \mathbf{Thrd}_{\text{exe}}^k$ ,  $\xrightarrow{\text{ax}}$  is a safe approximation of  $\xrightarrow{\text{ax}}$  (Lemma 5.49),  $\tilde{\mathbb{x}}^k$  contains safe write history, TRIM is safe (Lemma 5.27),  $\mathbf{Thrd}_{\tilde{c}^k} \subseteq \mathbf{Thrd}$  and AC-C-TIME is safe (Lemma 5.54), it must be that:

$$\begin{aligned}
 pc_{\mathsf{T}'} &= pc_{\mathsf{T}'}^{\tilde{c}} \wedge \\
 \mathbb{r}_{\mathsf{T}'} &\in \gamma_{\text{reg}}(\tilde{\mathbb{r}}_{\mathsf{T}'}) \wedge \\
 t_{\mathsf{T}'}^a &\in \gamma_t(\tilde{t}_{\mathsf{T}'}^a) \wedge \\
 \exists \mathbb{x}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}) : & (\forall x \in \mathbf{Var} : ((\mathbb{x} \ x) \mathsf{T}') \subseteq ((\mathbb{x}' \ x) \mathsf{T}')) \wedge \\
 \forall lck \in \mathbf{Lck} : & ((\text{OWN}(\mathbb{l}^0 \ lck) = \mathsf{T}' \vee \text{OWN}(\mathbb{l} \ lck) = \mathsf{T}') \Rightarrow \\
 & (\text{STT}(\mathbb{l} \ lck) = \text{sTT}(\tilde{\mathbb{l}} \ lck) \wedge \\
 & \text{OWN}(\mathbb{l} \ lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}} \ lck) \wedge \\
 & \text{DL}(\mathbb{l} \ lck) \in \gamma_t(\text{D}\tilde{\text{L}}(\tilde{\mathbb{l}} \ lck)) \wedge \\
 & \text{POWN}(\mathbb{l} \ lck) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}} \ lck) \wedge \\
 & \text{REL}(\mathbb{l} \ lck) \in \gamma_t(\text{R}\tilde{\text{E}}\text{L}(\tilde{\mathbb{l}} \ lck)) \wedge \\
 & \min(\gamma_t(\text{D}\tilde{\text{L}}(\tilde{\mathbb{l}} \ lck))) = -\infty))
 \end{aligned}$$

4. If, for some  $lck' \in \mathbf{Lck}$ ,  $\text{STM}(\mathsf{T}', pc_{\mathsf{T}'}^0) = [\text{lock } lck']^{\text{pc}_{\mathsf{T}'}}_0$ , only the case that  $\mathsf{T}'$  successfully and immediately acquires  $lck'$  needs to be considered. (Note that the remaining cases will be considered in the proofs of Lemmas 5.57 and 5.58.) Hence, AC-C-TIME is safe since it must be that  $\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^{k'} \ lck') = \mathsf{T}'$  and  $\text{OWN}(\mathbb{l}^{k'} \ lck') = \mathsf{T}'$  (Lemma 5.54).

Since  $\text{OWN}(\mathbb{l}^0 \ lck') = \mathsf{T}' \Rightarrow \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^0 \ lck') = \mathsf{T}'$  and  $\text{OWN}(\mathbb{l}^0 \ lck') = \perp_{\text{thrd}} \Rightarrow (\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^0 \ lck') = \perp_{\text{thrd}} \vee \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^0 \ lck') = \mathsf{T}')$ , there are three cases to consider.

- (a) Assume that  $\text{OWN}(\mathbb{l}^0 \ lck') = \mathsf{T}'$  (and thus,  $\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{l}}^0 \ lck') = \mathsf{T}'$ ) and let  $c @ \langle [\mathsf{T}, pc_{\mathsf{T}}, \mathbb{r}_{\mathsf{T}}, t_{\mathsf{T}}^a]_{\mathsf{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle$  be such that  $c^n \xrightarrow{\text{prg}} c$ . Then choose  $\tilde{c} @ \langle [\mathsf{T}, pc_{\mathsf{T}}^{\tilde{c}}, \tilde{\mathbb{r}}_{\mathsf{T}}, \tilde{t}_{\mathsf{T}}^a]_{\mathsf{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle$  such that  $\tilde{c}^k \xrightarrow{\text{prg}} \tilde{c}$ . It is

trivially the case that  $\text{OWN}(\mathbb{1} \text{ lck}') = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} \text{ lck}') = \text{T}'$  and thus

$$\begin{aligned}
 pc_{\text{T}'} &= pc_{\tilde{\text{T}}'}^{\tilde{c}} \wedge \\
 \mathbb{r}_{\text{T}'} &\in \gamma_{\text{reg}}(\tilde{\mathbb{r}}_{\text{T}'}) \wedge \\
 t_{\text{T}'}^a &\in \gamma_t(\tilde{t}_{\text{T}'})^a \wedge \\
 \exists \mathbb{x}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}) &: (\forall x \in \mathbf{Var} : ((\mathbb{x} \ x) \text{T}') \subseteq ((\mathbb{x}' \ x) \text{T}')) \wedge \\
 \forall \text{lck} \in \mathbf{Lck} &: ((\text{OWN}(\mathbb{1}^0 \text{ lck}) = \text{T}' \vee \text{OWN}(\mathbb{1} \text{ lck}) = \text{T}') \Rightarrow \\
 & \quad (\text{STT}(\mathbb{1} \text{ lck}) = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}} \text{ lck}) \wedge \\
 & \quad \text{OWN}(\mathbb{1} \text{ lck}) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} \text{ lck}) \wedge \\
 & \quad \text{DL}(\mathbb{1} \text{ lck}) \in \gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}} \text{ lck})) \wedge \\
 & \quad \text{POWN}(\mathbb{1} \text{ lck}) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} \text{ lck}) \wedge \\
 & \quad \text{REL}(\mathbb{1} \text{ lck}) \in \gamma_t(\tilde{\text{R}}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{1}} \text{ lck})) \wedge \\
 & \quad \min(\gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}} \text{ lck}))) = -\infty))
 \end{aligned}$$

since  $\forall i \in \{0, \dots, n-1\} : \text{T}' \notin \mathbf{Thrd}_{\text{exe}}^{c^i}$ ,  $\text{T}' \in \mathbf{Thrd}_{\text{exe}}^{c^n}$ ,  $\forall i \in \{0, \dots, k-1\} : \text{T}' \notin \mathbf{Thrd}_{\text{exe}}^{\tilde{c}^i}$ ,  $\text{T}' \in \mathbf{Thrd}_{\text{exe}}^{\tilde{c}^k}$ ,  $\xrightarrow{\tilde{c}^k}$  is a safe approximation of  $\xrightarrow{\tilde{c}^k}$  (Lemma 5.49) and TRIM is safe (Lemma 5.27).

- (b) Assume that  $\text{OWN}(\mathbb{1}^0 \text{ lck}') = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^0 \text{ lck}') = \perp_{\text{thrd}}$  and let  $c@ \langle [\text{T}, pc_{\text{T}}, \mathbb{r}_{\text{T}}, t_{\text{T}}^a]_{\text{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{1} \rangle$  be such that  $c^n \xrightarrow{\text{prg}} c \wedge \text{OWN}(\mathbb{1} \text{ lck}') = \text{T}'$  and choose  $\tilde{c}@ \langle [\text{T}, pc_{\tilde{\text{T}}}, \tilde{\mathbb{r}}_{\tilde{\text{T}}}, \tilde{t}_{\tilde{\text{T}}}^a]_{\text{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}, \tilde{\mathbb{1}} \rangle$  such that  $\tilde{c}^k \xrightarrow{\text{prg}} \tilde{c}$ .

Then it must be that  $\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} \text{ lck}') = \text{T}'$  (since  $\text{T}' \in \mathbf{Thrd}_{\text{exe}}^{\tilde{c}^k}$  and thus  $\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^{k'} \text{ lck}') = \text{T}'$ ) and

$$\begin{aligned}
 pc_{\text{T}'} &= pc_{\tilde{\text{T}}'}^{\tilde{c}} \wedge \\
 \mathbb{r}_{\text{T}'} &\in \gamma_{\text{reg}}(\tilde{\mathbb{r}}_{\text{T}'}) \wedge \\
 t_{\text{T}'}^a &\in \gamma_t(\tilde{t}_{\text{T}'})^a \wedge \\
 \exists \mathbb{x}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}) &: (\forall x \in \mathbf{Var} : ((\mathbb{x} \ x) \text{T}') \subseteq ((\mathbb{x}' \ x) \text{T}')) \wedge \\
 \forall \text{lck} \in \mathbf{Lck} &: ((\text{OWN}(\mathbb{1}^0 \text{ lck}) = \text{T}' \vee \text{OWN}(\mathbb{1} \text{ lck}) = \text{T}') \Rightarrow \\
 & \quad (\text{STT}(\mathbb{1} \text{ lck}) = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}} \text{ lck}) \wedge \\
 & \quad \text{OWN}(\mathbb{1} \text{ lck}) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} \text{ lck}) \wedge \\
 & \quad \text{DL}(\mathbb{1} \text{ lck}) \in \gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}} \text{ lck})) \wedge \\
 & \quad \text{POWN}(\mathbb{1} \text{ lck}) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} \text{ lck}) \wedge \\
 & \quad \text{REL}(\mathbb{1} \text{ lck}) \in \gamma_t(\tilde{\text{R}}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{1}} \text{ lck})) \wedge \\
 & \quad \min(\gamma_t(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}} \text{ lck}))) = -\infty))
 \end{aligned}$$

since  $\forall i \in \{0, \dots, n-1\} : \text{T}' \notin \mathbf{Thrd}_{\text{exe}}^{c^i}$ ,  $\text{T}' \in \mathbf{Thrd}_{\text{exe}}^{c^n}$ ,  $\forall i \in \{0, \dots, k-1\} : \text{T}' \notin \mathbf{Thrd}_{\text{exe}}^{\tilde{c}^i}$ ,  $\text{T}' \in \mathbf{Thrd}_{\text{exe}}^{\tilde{c}^k}$ ,  $\xrightarrow{\tilde{c}^k}$  is a safe approxi-

mation of  $\xrightarrow{ax}$  (Lemma 5.49), TRIM is safe (Lemma 5.27),  $\mathbf{Thrd}_{\check{c}^k} \subseteq \mathbf{Thrd}$ ,  $\forall \check{c}' \in \mathbf{C\ddot{o}nf} : \forall lck \in \mathbf{Lck} : \min(\text{DLLOCK}(\check{c}', lck)) = -\infty$  (Algorithm 5.11),  $\text{DL}(\mathbb{1} lck') = t_{T'}^a = t_{T'}^{a^n} + \text{TIME}(c^n, T')$  (Table 4.3) and  $t_{T'}^a \in \gamma_t(\text{DLLOCK}(\check{c}^k, lck'))$  (Lemma 5.53).

- (c) Assume that  $\text{OWN}(\mathbb{1}^0 lck') = \perp_{\text{thrd}}$  and  $\text{O}\check{\text{W}}\text{N}(\check{\mathbb{1}}^0 lck') = T'$  and let  $c @ \langle [T, pc_T, \mathbb{r}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{1} \rangle$  be such that  $c^n \xrightarrow{\text{prg}} c \wedge \text{OWN}(\mathbb{1} lck') = T'$  and choose  $\check{c} @ \langle [T, pc_{\check{T}}, \check{\mathbb{r}}_T, \check{t}_T^a]_{T \in \mathbf{Thrd}_{\check{c}^k}}, \check{\mathbb{x}}, \check{\mathbb{1}} \rangle$  such that  $\check{c}^k \xrightarrow{\text{prg}} \check{c}$ . Then it is easy to see that  $\text{OWN}(\mathbb{1} lck') = \text{O}\check{\text{W}}\text{N}(\check{\mathbb{1}} lck') = T'$ .

First note that since  $\text{OWN}(\mathbb{1}^n lck') = \text{OWN}(\mathbb{1}^0 lck') = \perp_{\text{thrd}} \wedge \text{O}\check{\text{W}}\text{N}(\check{\mathbb{1}}^k lck') = \text{O}\check{\text{W}}\text{N}(\check{\mathbb{1}}^0 lck') = T'$ , it must be that  $\text{STT}(\mathbb{1}^n lck') = \text{S}\check{\text{T}}\text{T}(\check{\mathbb{1}}^k lck') = \text{S}\check{\text{T}}\text{T}(\check{\mathbb{1}}^0 lck') = \text{unlocked}$ ,  $\check{\text{D}}\check{\text{L}}(\check{\mathbb{1}} lck') = \check{\text{D}}\check{\text{L}}(\check{\mathbb{1}}^{k''} lck') = \check{\text{D}}\check{\text{L}}(\check{\mathbb{1}}^k lck') = \check{\text{D}}\check{\text{L}}(\check{\mathbb{1}}^0 lck')$ , and thus  $\min(\gamma_t(\check{\text{D}}\check{\text{L}}(\check{\mathbb{1}} lck'))) = -\infty$  and  $t_{T'}^{a^n} + \text{TIME}(c^n, T') \in \gamma_t(\check{\text{D}}\check{\text{L}}(\check{\mathbb{1}} lck'))$ , which means that  $\text{DL}(\check{\mathbb{1}} lck') \in \gamma_t(\check{\text{D}}\check{\text{L}}(\check{\mathbb{1}} lck'))$  since  $\text{DL}(\check{\mathbb{1}} lck') = t_{T'}^{a^n} + \text{TIME}(c^n, T')$ .

Note that since  $t_{T'}^{a^n} \in \gamma_t(\check{t}_{T'}^{a^k})$ , it must be that  $\check{\text{D}}\check{\text{L}}(\check{\mathbb{1}}^{k''} lck') \check{\gamma}_t \check{t}_{T'}^{a^k} \check{\ddagger}_t \text{ABSTIME}(\check{c}^k, T')$ . It is thus easy to see that

$$\begin{aligned}
 pc_{T'} &= pc_{\check{T}'} \wedge \\
 \mathbb{r}_{T'} &\in \gamma_{\text{reg}}(\check{\mathbb{r}}_{T'}) \wedge \\
 t_{T'}^a &\in \gamma_t(\check{t}_{T'}^a) \wedge \\
 \exists \mathbb{x}' \in \gamma_{\text{var}}(\check{\mathbb{x}}) : &(\forall x \in \mathbf{Var} : ((\mathbb{x} x) T') \subseteq ((\mathbb{x}' x) T')) \wedge \\
 \forall lck \in \mathbf{Lck} : &((\text{OWN}(\mathbb{1}^0 lck) = T' \vee \text{OWN}(\mathbb{1} lck) = T') \Rightarrow \\
 &(\text{STT}(\mathbb{1} lck) = \text{S}\check{\text{T}}\text{T}(\check{\mathbb{1}} lck) \wedge \\
 &\text{OWN}(\mathbb{1} lck) = \text{O}\check{\text{W}}\text{N}(\check{\mathbb{1}} lck) \wedge \\
 &\text{DL}(\mathbb{1} lck) \in \gamma_t(\check{\text{D}}\check{\text{L}}(\check{\mathbb{1}} lck)) \wedge \\
 &\text{POWN}(\mathbb{1} lck) = \text{PO}\check{\text{W}}\text{N}(\check{\mathbb{1}} lck) \wedge \\
 &\text{REL}(\mathbb{1} lck) \in \gamma_t(\check{\text{R}}\check{\text{E}}\check{\text{L}}(\check{\mathbb{1}} lck)) \wedge \\
 &\min(\gamma_t(\check{\text{D}}\check{\text{L}}(\check{\mathbb{1}} lck))) = -\infty))
 \end{aligned}$$

since  $\forall i \in \{0, \dots, n-1\} : T' \notin \mathbf{Thrd}_{\text{exe}}^i$ ,  $T' \in \mathbf{Thrd}_{\text{exe}}^n$ ,  $\forall i \in \{0, \dots, k-1\} : T' \notin \mathbf{Thrd}_{\text{exe}}^i$ ,  $T' \in \mathbf{Thrd}_{\text{exe}}^k$ ,  $\xrightarrow{ax}$  is a safe approximation of  $\xrightarrow{ax}$  (Lemma 5.49), TRIM is safe (Lemma 5.27) and

$\mathbf{Thrd}_{\check{c}^k} \subseteq \mathbf{Thrd}$ .

This concludes the proof. ■



Lemma 5.57 shows that  $\xrightarrow[\text{prg}]{\sim}$  safely approximates the case that a thread issuing `lock lck` for some lock,  $lck \in \mathbf{Lck}$ , has to wait for an arbitrary number of owner switches on  $lck$  before it acquires  $lck$ . Note that the lemma holds if all threads wanting to acquire some lock eventually will be able to do so (which obviously is the case if the concrete transition sequences are finite in length) and if either no thread issues a `load`-statement on a global variable or that the thread issuing the `load`-statement is the sole thread in  $\mathbf{Thrd}_{\text{exe}}$  in any step of the transition sequence.

**Lemma 5.57 (Soundness of  $\xrightarrow[\text{prg}]{\sim}$ , frozen thread):**

Given the valid concrete configurations (c.f., Definition 4.4), abstract configurations, lock and thread

$$\begin{aligned}
 & c^0 @ \langle [\mathbf{T}, pc_{\mathbf{T}}^0, \mathbb{x}_{\mathbf{T}}^0, t_{\mathbf{T}}^{a^0}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^0, \mathbb{l}^0 \rangle \in \mathbf{Conf}, \\
 & c^{n_1} @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{n_1}, \mathbb{x}_{\mathbf{T}}^{n_1}, t_{\mathbf{T}}^{a^{n_1}}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^{n_1}, \mathbb{l}^{n_1} \rangle \in \mathbf{Conf}, \\
 & c^{n_2} @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{n_2}, \mathbb{x}_{\mathbf{T}}^{n_2}, t_{\mathbf{T}}^{a^{n_2}}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^{n_2}, \mathbb{l}^{n_2} \rangle \in \mathbf{Conf}, \\
 & \quad \vdots \\
 & c^{n_m} @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{n_m}, \mathbb{x}_{\mathbf{T}}^{n_m}, t_{\mathbf{T}}^{a^{n_m}}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^{n_m}, \mathbb{l}^{n_m} \rangle \in \mathbf{Conf}, \\
 & c^n @ \langle [\mathbf{T}, pc_{\mathbf{T}}^n, \mathbb{x}_{\mathbf{T}}^n, t_{\mathbf{T}}^{a^n}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^n, \mathbb{l}^n \rangle \in \mathbf{Conf}, \\
 & \tilde{c}^0 @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^0}, \tilde{\mathbb{x}}_{\mathbf{T}}^0, \tilde{t}_{\mathbf{T}}^{a^0}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^0}}, \tilde{\mathbb{x}}^0, \tilde{\mathbb{l}}^0 \rangle \in \mathbf{C\~{o}nf}, \\
 & \tilde{c}^k @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^k}, \tilde{\mathbb{x}}_{\mathbf{T}}^k, \tilde{t}_{\mathbf{T}}^{a^k}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}^k, \tilde{\mathbb{l}}^k \rangle \in \mathbf{C\~{o}nf}, \\
 & lck' \in \mathbf{Lck}, \text{ and} \\
 & \mathbf{T}' \in \mathbf{Thrd}_{\tilde{c}^k},
 \end{aligned}$$

such that

$$\begin{aligned}
 & \text{STM}(\mathbf{T}', pc_{\mathbf{T}'}^0) = [\text{lock } lck']^{pc_{\mathbf{T}'}^0}, \\
 & 0 \leq n_1 \leq n_2 \leq n_m \leq n, \\
 & c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n_1} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n_2} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n_m} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n, \\
 & 0 \leq k, \\
 & \tilde{c}^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^k, \\
 & \mathbf{Thrd}_{\tilde{c}^k} \subseteq \mathbf{Thrd}_{\tilde{c}^0} \subseteq \mathbf{Thrd}, \\
 & pc_{\mathbf{T}'}^0 = pc_{\tilde{\mathbf{T}}'}^0, \\
 & \mathbb{I}_{\mathbf{T}'}^0 \in \gamma_{\text{reg}}(\tilde{\mathbb{I}}_{\mathbf{T}'}^0), \\
 & t_{\mathbf{T}'}^{a^0} \in \gamma_t(\tilde{t}_{\mathbf{T}'}^{a^0}), \\
 & \exists \mathbf{x}' \in \gamma_{\text{var}}(\tilde{\mathbf{x}}^0) : \forall x \in \mathbf{Var} : \forall \mathbf{T} \in \mathbf{Thrd} : ((\mathbf{x}^0 x) \mathbf{T}) \subseteq ((\mathbf{x}' x) \mathbf{T}), \\
 & \forall lck \in \mathbf{Lck} : ((\text{OWN}(\mathbb{I}^0 lck) \neq \perp_{\text{thrd}} \Rightarrow (\text{STT}(\mathbb{I}^0 lck) = \text{STT}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \text{OWN}(\mathbb{I}^0 lck) = \text{OWN}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \text{DL}(\mathbb{I}^0 lck) \in \gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \text{POWN}(\mathbb{I}^0 lck) = \text{POWN}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \text{REL}(\mathbb{I}^0 lck) \in \gamma_t(\tilde{\text{REL}}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 lck))) = -\infty)) \wedge \\
 & (\text{OWN}(\mathbb{I}^0 lck) = \perp_{\text{thrd}} \Rightarrow ((\text{OWN}(\mathbb{I}^0 lck) = \text{OWN}(\tilde{\mathbb{I}}^0 lck) \vee \\
 & \quad (\text{OWN}(\tilde{\mathbb{I}}^0 lck) = \mathbf{T}' \wedge \\
 & \quad \text{STT}(\tilde{\mathbb{I}}^0 lck) = \text{unlocked} \wedge \\
 & \quad t_{\mathbf{T}'}^{a^n} + \text{TIME}(c^n, \mathbf{T}') \in \gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 lck))) = -\infty)) \wedge \\
 & \quad \text{POWN}(\mathbb{I}^0 lck) = \text{POWN}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \text{REL}(\mathbb{I}^0 lck) \in \gamma_t(\tilde{\text{REL}}(\tilde{\mathbb{I}}^0 lck))))), \\
 & \forall i \in \{0, \dots, n-1\} \setminus \{n_1, n_2, \dots, n_m\} : \mathbf{T}' \notin \mathbf{Thrd}_{\text{exe}}^i, \\
 & \forall i \in \{n_1, n_2, \dots, n_m\} : (\mathbf{T}' \in \mathbf{Thrd}_{\text{exe}}^i \wedge \text{OWN}(\mathbb{I}^{i'} lck') \neq \mathbf{T}'), \\
 & \quad \mathbf{T}' \in \mathbf{Thrd}_{\text{exe}}^n, \\
 & \forall i \in \{0, \dots, k-1\} : \mathbf{T}' \notin \mathbf{Thrd}_{\text{exe}}^i, \\
 & \quad \mathbf{T}' \in \mathbf{Thrd}_{\text{exe}}^k, \text{ and} \\
 & \forall i \in \{0, \dots, k\} : (|\mathbf{Thrd}_{\text{exe}}^i| \neq 1 \vee \\
 & \quad \{\mathbf{T} \in \mathbf{Thrd}_{\text{exe}}^i \mid \exists r \in \mathbf{Reg}_{\mathbf{T}} : \exists x \in \mathbf{Var}_{\mathbf{g}} : \\
 & \quad \quad \text{STM}(\mathbf{T}, pc_{\mathbf{T}}^i) = [\text{load } r \text{ from } x]^{pc_{\mathbf{T}}^i} = \emptyset),
 \end{aligned}$$

where for all  $i \in \{0, \dots, n\}$ ,  $\mathbf{Thrd}_{\text{exe}}^i$  is as defined in Table 4.3, for all  $i \in \{0, \dots, k\}$ ,  $\mathbf{Thrd}_{\text{exe}}^i$  is as defined in Table 5.6, and  $\mathbf{Var}_{\mathbf{g}}$  contains all  $x \in \mathbf{Var}$  such that  $x$  can be written to by one thread and read from by another thread

(i.e., there might be a data dependency between the threads; note that  $\mathbf{Var}_g$  can be derived using Algorithm 6.9),  $\xrightarrow{\text{prg}}$  satisfies:

$$\begin{aligned}
 & \forall c @ \langle [\mathbf{T}, pc_{\mathbf{T}}, \mathbb{r}_{\mathbf{T}}, t_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf} : \\
 & (c^n \xrightarrow{\text{prg}} c \Rightarrow \exists \tilde{c} @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}}, \tilde{\mathbb{r}}_{\mathbf{T}}, \tilde{t}_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \mathbf{C\tilde{on}f} : \\
 & \quad (\tilde{c}^k \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c} \wedge \\
 & \quad pc_{\mathbf{T}'} = pc_{\mathbf{T}'}^{\tilde{c}} \wedge \\
 & \quad \mathbb{r}_{\mathbf{T}'} \in \gamma_{\text{reg}}(\tilde{\mathbb{r}}_{\mathbf{T}'}) \wedge \\
 & \quad t_{\mathbf{T}'}^a \in \gamma_t(\tilde{t}_{\mathbf{T}'}^a) \wedge \\
 & \quad \exists \mathbb{x}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}) : (\forall x \in \mathbf{Var} : ((\mathbb{x} \ x) \mathbf{T}') \subseteq ((\mathbb{x}' \ x) \mathbf{T}')) \wedge \\
 & \quad \forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{l} \ lck) = \mathbf{T}' \Rightarrow (\text{STT}(\mathbb{l} \ lck) = \text{STT}(\tilde{\mathbb{l}} \ lck) \wedge \\
 & \quad \text{OWN}(\mathbb{l} \ lck) = \text{OWN}(\tilde{\mathbb{l}} \ lck) \wedge \\
 & \quad \text{DL}(\mathbb{l} \ lck) \in \gamma_t(\text{DL}(\tilde{\mathbb{l}} \ lck)) \wedge \\
 & \quad \text{POWN}(\mathbb{l} \ lck) = \text{POWN}(\tilde{\mathbb{l}} \ lck) \wedge \\
 & \quad \text{REL}(\mathbb{l} \ lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{l}} \ lck)) \wedge \\
 & \quad \min(\gamma_t(\text{DL}(\tilde{\mathbb{l}} \ lck))) = -\infty))) \quad \square
 \end{aligned}$$

PROOF. Assume that the valid concrete configurations (c.f., Definition 4.4), abstract configurations, lock and thread

$$\begin{aligned}
 & c^0 @ \langle [\mathbf{T}, pc_{\mathbf{T}}^0, \mathbb{r}_{\mathbf{T}}^0, t_{\mathbf{T}}^{a^0}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^0, \mathbb{l}^0 \rangle \in \mathbf{Conf}, \\
 & c^{n_1} @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{n_1}, \mathbb{r}_{\mathbf{T}}^{n_1}, t_{\mathbf{T}}^{a^{n_1}}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^{n_1}, \mathbb{l}^{n_1} \rangle \in \mathbf{Conf}, \\
 & c^{n_2} @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{n_2}, \mathbb{r}_{\mathbf{T}}^{n_2}, t_{\mathbf{T}}^{a^{n_2}}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^{n_2}, \mathbb{l}^{n_2} \rangle \in \mathbf{Conf}, \\
 & \quad \vdots \\
 & c^{n_m} @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{n_m}, \mathbb{r}_{\mathbf{T}}^{n_m}, t_{\mathbf{T}}^{a^{n_m}}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^{n_m}, \mathbb{l}^{n_m} \rangle \in \mathbf{Conf}, \\
 & c^n @ \langle [\mathbf{T}, pc_{\mathbf{T}}^n, \mathbb{r}_{\mathbf{T}}^n, t_{\mathbf{T}}^{a^n}]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}^n, \mathbb{l}^n \rangle \in \mathbf{Conf}, \\
 & \tilde{c}^0 @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^0}, \tilde{\mathbb{r}}_{\mathbf{T}}^0, \tilde{t}_{\mathbf{T}}^{a^0}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^0}}, \tilde{\mathbb{x}}^0, \tilde{\mathbb{l}}^0 \rangle \in \mathbf{C\tilde{on}f}, \\
 & \tilde{c}^k @ \langle [\mathbf{T}, pc_{\mathbf{T}}^{\tilde{c}^k}, \tilde{\mathbb{r}}_{\mathbf{T}}^k, \tilde{t}_{\mathbf{T}}^{a^k}]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}^k}}, \tilde{\mathbb{x}}^k, \tilde{\mathbb{l}}^k \rangle \in \mathbf{C\tilde{on}f}, \\
 & lck' \in \mathbf{Lck}, \text{ and} \\
 & \mathbf{T}' \in \mathbf{Thrd}_{\tilde{c}^k},
 \end{aligned}$$

are such that

$$\begin{aligned}
 & \text{STM}(\mathbf{T}', pc_{\mathbf{T}'}^0) = [\text{lock } lck']^{pc_{\mathbf{T}'}^0}, \\
 & 0 \leq n_1 \leq n_2 \leq n_m \leq n, \\
 & c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n_1} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n_2} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n_m} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n, \\
 & 0 \leq k, \\
 & \tilde{c}^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^k, \\
 & \mathbf{Thrd}_{\tilde{c}^k} \subseteq \mathbf{Thrd}_{\tilde{c}^0} \subseteq \mathbf{Thrd}, \\
 & pc_{\mathbf{T}'}^0 = pc_{\tilde{\mathbf{T}}'}^0, \\
 & \mathbb{I}_{\mathbf{T}'}^0 \in \gamma_{\text{reg}}(\tilde{\mathbb{I}}_{\mathbf{T}'}^0), \\
 & t_{\mathbf{T}'}^{a^0} \in \gamma_t(\tilde{t}_{\mathbf{T}'}^{a^0}), \\
 & \exists \mathbf{x}' \in \gamma_{\text{var}}(\tilde{\mathbf{x}}^0) : \forall x \in \mathbf{Var} : \forall \mathbf{T} \in \mathbf{Thrd} : ((\mathbf{x}^0 x) \mathbf{T}) \subseteq ((\mathbf{x}' x) \mathbf{T}), \\
 & \forall lck \in \mathbf{Lck} : ((\text{OWN}(\mathbb{I}^0 lck) \neq \perp_{\text{thrd}} \Rightarrow (\text{STT}(\mathbb{I}^0 lck) = \text{STT}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \text{OWN}(\mathbb{I}^0 lck) = \text{OWN}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \text{DL}(\mathbb{I}^0 lck) \in \gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \text{POWN}(\mathbb{I}^0 lck) = \text{POWN}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \text{REL}(\mathbb{I}^0 lck) \in \gamma_t(\tilde{\text{REL}}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 lck))) = -\infty)) \wedge \\
 & (\text{OWN}(\mathbb{I}^0 lck) = \perp_{\text{thrd}} \Rightarrow ((\text{OWN}(\mathbb{I}^0 lck) = \text{OWN}(\tilde{\mathbb{I}}^0 lck) \vee \\
 & \quad (\text{OWN}(\tilde{\mathbb{I}}^0 lck) = \mathbf{T}' \wedge \\
 & \quad \text{STT}(\tilde{\mathbb{I}}^0 lck) = \text{unlocked} \wedge \\
 & \quad t_{\mathbf{T}'}^{a^n} + \text{TIME}(c^n, \mathbf{T}') \in \gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
 & \quad \min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 lck))) = -\infty)) \wedge \\
 & \quad \text{POWN}(\mathbb{I}^0 lck) = \text{POWN}(\tilde{\mathbb{I}}^0 lck) \wedge \\
 & \quad \text{REL}(\mathbb{I}^0 lck) \in \gamma_t(\tilde{\text{REL}}(\tilde{\mathbb{I}}^0 lck))))), \\
 & \forall i \in \{0, \dots, n-1\} \setminus \{n_1, n_2, \dots, n_m\} : \mathbf{T}' \notin \mathbf{Thrd}_{\text{exe}}^i, \\
 & \forall i \in \{n_1, n_2, \dots, n_m\} : (\mathbf{T}' \in \mathbf{Thrd}_{\text{exe}}^i \wedge \text{OWN}(\mathbb{I}^{i'} lck') \neq \mathbf{T}'), \\
 & \quad \mathbf{T}' \in \mathbf{Thrd}_{\text{exe}}^n, \\
 & \forall i \in \{0, \dots, k-1\} : \mathbf{T}' \notin \mathbf{Thrd}_{\text{exe}}^i, \\
 & \quad \mathbf{T}' \in \mathbf{Thrd}_{\text{exe}}^k, \text{ and} \\
 & \forall i \in \{0, \dots, k\} : (|\mathbf{Thrd}_{\text{exe}}^i| \neq 1 \vee \\
 & \quad \{\mathbf{T} \in \mathbf{Thrd}_{\text{exe}}^i \mid \exists r \in \mathbf{Reg}_{\mathbf{T}} : \exists x \in \mathbf{Var}_{\mathbf{g}} : \\
 & \quad \quad \text{STM}(\mathbf{T}, pc_{\mathbf{T}}^i) = [\text{load } r \text{ from } x]^{pc_{\mathbf{T}}^i} = \emptyset),
 \end{aligned}$$

where for all  $i \in \{0, \dots, n\}$ ,  $\mathbf{Thrd}_{\text{exe}}^i$  is as defined in Table 4.3, for all  $i \in \{0, \dots, k\}$ ,  $\mathbf{Thrd}_{\text{exe}}^i$  is as defined in Table 5.6, and  $\mathbf{Var}_{\mathbf{g}}$  contains all  $x \in \mathbf{Var}$  such that  $x$  can be written to by one thread and read from by another thread

(i.e., there might be a data dependency between the threads; note that  $\mathbf{Var}_g$  can be derived using Algorithm 6.9).

First note that:

- Since  $\forall i \in \{0, \dots, n-1\} \setminus \{n_1, n_2, \dots, n_m\} : T' \notin \mathbf{Thrd}_{exe}^i$ ,  $\forall i \in \{n_1, n_2, \dots, n_m\} : (T' \in \mathbf{Thrd}_{exe}^i \wedge \text{OWN}(\mathbb{1}^{i'} lck') \neq T')$  and  $\text{STM}(T', pc_{T'}^0) = [\text{lock } lck']^{pc_{T'}^0}$ , it must be that  $pc_{T'}^n = pc_{T'}^0$ ,  $\mathbb{r}_{T'}^n = \mathbb{r}_{T'}^0$ ,  $t_{T'}^n = t_{T'}^0 + \text{TIME}(c^{n_1}, T') + \text{TIME}(c^{n_2}, T') + \dots + \text{TIME}(c^{n_m}, T')$  and  $\forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{1}^0 lck) = T' \Rightarrow \mathbb{1}^n lck = \mathbb{1}^0 lck)$  (c.f., Table 4.3).

- Since  $\forall i \in \{0, \dots, k-1\} : T' \notin \mathbf{Thrd}_{exe}^i$ , it must be that  $pc_{T'}^k = pc_{T'}^0$ ,  $\tilde{\mathbb{r}}_{T'}^k = \tilde{\mathbb{r}}_{T'}^0$ ,  $\tilde{t}_{T'}^k = \tilde{t}_{T'}^0$  and  $\forall lck \in \mathbf{Lck} : (\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^0 lck) = T' \Rightarrow (\tilde{\mathbb{1}}^k lck = \tilde{\mathbb{1}}^0 lck \wedge \min(\gamma_i(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}}^k lck))) = -\infty))$ .

- Since  $pc_{T'}^n = pc_{T'}^0$ ,  $\mathbb{r}_{T'}^n = \mathbb{r}_{T'}^0$ ,  $\forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{1}^0 lck) = T' \Rightarrow \mathbb{1}^n lck = \mathbb{1}^0 lck)$ ,  $pc_{T'}^k = pc_{T'}^0$ ,  $\tilde{\mathbb{r}}_{T'}^k = \tilde{\mathbb{r}}_{T'}^0$ ,  $\forall lck \in \mathbf{Lck} : (\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^0 lck) = T' \Rightarrow (\tilde{\mathbb{1}}^k lck = \tilde{\mathbb{1}}^0 lck \wedge \min(\gamma_i(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}}^k lck))) = -\infty))$ ,  $pc_{T'}^0 = pc_{T'}^0$ ,  $\mathbb{r}_{T'}^0 \in \gamma_{\text{reg}}(\tilde{\mathbb{r}}_{T'}^0)$ ,  $t_{T'}^0 \in \gamma_i(\tilde{t}_{T'}^0)$  and  $\forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{1}^0 lck) = T' \Rightarrow (\text{STT}(\mathbb{1}^0 lck) = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}}^0 lck) \wedge \text{OWN}(\mathbb{1}^0 lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^0 lck) \wedge \text{DL}(\mathbb{1}^0 lck) \in \gamma_i(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}}^0 lck)) \wedge \text{POWN}(\mathbb{1}^0 lck) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^0 lck) \wedge \text{REL}(\mathbb{1}^0 lck) \in \gamma_i(\tilde{\text{R}}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{1}}^0 lck)) \wedge \min(\gamma_i(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}}^0 lck))) = -\infty))$ , it must be that:

$$\begin{aligned}
 pc_{T'}^n &= pc_{T'}^k, \\
 \mathbb{r}_{T'}^n &\in \gamma_{\text{reg}}(\tilde{\mathbb{r}}_{T'}^k) \text{ and} \\
 \forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{1}^n lck) = T' \Rightarrow &(\text{STT}(\mathbb{1}^n lck) = \text{S}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}}^k lck) \wedge \\
 &\text{OWN}(\mathbb{1}^n lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^k lck) \wedge \\
 &\text{DL}(\mathbb{1}^n lck) \in \gamma_i(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}}^k lck)) \wedge \\
 &\text{POWN}(\mathbb{1}^n lck) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^k lck) \wedge \\
 &\text{REL}(\mathbb{1}^n lck) \in \gamma_i(\tilde{\text{R}}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{1}}^k lck)) \wedge \\
 &\min(\gamma_i(\tilde{\text{D}}\tilde{\text{L}}(\tilde{\mathbb{1}}^k lck))) = -\infty))
 \end{aligned}$$

- Since  $\exists x' \in \gamma_{\text{var}}(\tilde{x}^0) : \forall x \in \mathbf{Var} : ((x^0 x) T') \subseteq ((x' x) T')$ ,  $c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n_1} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n_2} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n_m} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n$ ,  $\tilde{c}^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^k$ ,  $\forall i \in \{0, \dots, n-1\} \setminus \{n_1, n_2, \dots, n_m\} : T' \notin \mathbf{Thrd}_{exe}^i$ ,  $\forall i \in \{n_1, n_2, \dots, n_m\} : \text{OWN}(\mathbb{1}^{i'} lck') \neq T'$ ,  $\forall i \in \{0, \dots, k-1\} : T' \notin \mathbf{Thrd}_{exe}^i$ ,  $\text{STM}(T', pc_{T'}^0) = [\text{lock } lck']^{pc_{T'}^0}$  and  $\text{TRIM}$  is safe (Lemma 5.27), it must be that  $\exists x' \in \gamma_{\text{var}}(\tilde{x}^k) : \forall x \in \mathbf{Var} : ((x^n x) T') \subseteq ((x' x) T')$ .

- Since  $\forall i \in \{0, \dots, k\} : (|\mathbf{Thrd}_{exe}^{ci}| \not\approx 1 \vee \{\mathbf{T} \in \mathbf{Thrd}_{exe}^{ci} \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : \text{STM}(\mathbf{T}, pc_T^{ci}) = [\text{load } r \text{ from } x]^{pc_T^{ci}}\} = \emptyset)$ , it must be that  $\forall i \in \{0, \dots, k\} : (\{\mathbf{T} \in \mathbf{Thrd}_{exe}^{ci} \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : \text{STM}(\mathbf{T}, pc_T^{ci}) = [\text{load } r \text{ from } x]^{pc_T^{ci}}\} \neq \emptyset \Rightarrow |\mathbf{Thrd}_{exe}^{ci}| = 1)$ . This means that if some thread in  $\mathbf{Thrd}_{exe}^{ci}$ , where  $i \in \{0, \dots, k\}$ , performs a load-statement, there is only one single thread in  $\mathbf{Thrd}_{exe}^{ci}$ ; thus that thread performs the load-statement. It is then easy to see, from the definition of  $\mathbf{Thrd}_{exe}^{ci}$ , that there cannot occur any other write than those represented by  $\tilde{x}^i$  such that it could affect the load-statement of the thread in  $\mathbf{Thrd}_{exe}^{ci}$  (c.f., Assumption 5.50) – thus, it must be that  $\tilde{x}^k$  (and also all  $\tilde{x}^i$ , where  $i \in \{0, \dots, k\}$ ) contains safe write history (c.f., Definition 5.18).
- Since, trivially,  $\forall lck \in \mathbf{Lck} : \{\mathbf{T} \in \mathbf{Thrd}_{exe}^{cn} \cap \mathbf{Thrd}_{ck} \mid \text{STM}(\mathbf{T}, pc_T^n) = [\text{lock } lck]^{pc_T^n}\} \subseteq \{\mathbf{T} \in \mathbf{Thrd}_{ck} \mid \exists l \in \mathbf{Lbl}_T : \text{STM}(\mathbf{T}, l) = [\text{lock } lck]^l\}$ , it must be that if  $T'$  can be assigned a lock in the concrete case, it can also be assigned the lock in the corresponding abstract case.
- Since  $\xrightarrow{prg}$  over-approximates the lock-owner assignment possible for  $\xrightarrow{prg}$  and  $T' \in \mathbf{Thrd}_{ck}$ , it must be that  $\text{OWN}(\tilde{\mathbb{I}}^0 lck') = T'$  is possible even if  $\text{OWN}(\mathbb{I}^0 lck') = \perp_{thrd}$ , given that some other thread (i.e., not  $T'$ ) does  $\text{lock } lck'$  before  $T'$  in the abstract case and that the abstract transition sequence safely represents the concrete transition sequence; the situation is possible since  $\mathbf{Time} = \mathbf{Intv}$  (c.f., Lemma 5.55). However, if  $\text{STM}(T', pc_{T'}^0) = [\text{lock } lck']^{pc_{T'}^0}$ ,  $\text{OWN}(\mathbb{I}^0 lck') = \perp_{thrd}$  and  $\text{OWN}(\tilde{\mathbb{I}}^0 lck') = T'$ , it must be that  $\text{STT}(\tilde{\mathbb{I}}^0 lck') = \text{unlocked}$ ,  $t_{T'}^{cn} + \text{TIME}(c^n, T') \in \gamma_t(\text{DL}(\tilde{\mathbb{I}}^0 lck'))$  and  $\min(\gamma_t(\text{DL}(\tilde{\mathbb{I}}^0 lck'))) = -\infty$  (Table 5.6, Algorithm 5.11 and Lemmas 5.53 and 5.55).
- Since  $\text{STM}(T', pc_{T'}^{ck}) = [\text{lock } lck']^{pc_{T'}^{ck}}$  and  $T' \in \mathbf{Thrd}_{exe}^{ck}$ , it must be that  $\text{OWN}(\tilde{\mathbb{I}}^{k''} lck') = T'$ .

The proof will be conducted using induction based on  $T'$  having to wait for  $j$ , where  $j \geq 0$ , threads to first (acquire and) release  $lck'$  before it can successfully acquire  $lck'$ .

First consider the base case. Therefore, assume that  $T'$  is the first thread in a set of competing threads to successfully acquire  $lck'$ ; i.e.,  $j = 0$ . Then it must be that  $\{n_1, n_2, \dots, n_m\} = \emptyset$ , and thus,  $\forall i \in \{0, \dots, n-1\} : T' \notin \mathbf{Thrd}_{exe}^{ci}$ . (Note

that  $c^0$  can be chosen to be the first configuration satisfying  $\text{OWN}(\mathbb{1}^0 lck') = \perp_{\text{thrd}} \wedge \text{STM}(\mathbb{T}', pc_{\mathbb{T}'}^0) = [\text{lock } lck']^{pc_{\mathbb{T}'}^0}$  and the rest of the assumptions of the lemma.) It must also be that the case  $\text{OWN}(\mathbb{1}^n lck') = \perp_{\text{thrd}}$ ,  $\text{O}\check{\text{W}}\text{N}(\tilde{\mathbb{1}}^k lck') \in \{\perp_{\text{thrd}}, \mathbb{T}'\}$  and  $\text{OWN}(\mathbb{1}^{n''} lck') = \text{O}\check{\text{W}}\text{N}(\tilde{\mathbb{1}}^{k''} lck') = \mathbb{T}'$  must be considered.

Since  $\mathbb{T}'$  is the first thread to acquire  $lck'$  it must be that  $\mathbb{1}^n lck' = \mathbb{1}^0 lck'$  and  $\tilde{\mathbb{1}}^k lck' = \tilde{\mathbb{1}}^0 lck'$ . Thus, since  $\text{OWN}(\mathbb{1}^0 lck') = \perp_{\text{thrd}}$  and  $\text{STM}(\mathbb{T}', pc_{\mathbb{T}'}^0) = [\text{lock } lck']^{pc_{\mathbb{T}'}^0}$ , it must be that  $\text{OWN}(\mathbb{1}^0 lck') = \perp_{\text{thrd}} \Rightarrow (\text{STM}(\mathbb{T}', pc_{\mathbb{T}'}^0) = [\text{lock } lck']^{pc_{\mathbb{T}'}^0} \Rightarrow (\mathbb{1}^n lck' = \mathbb{1}^0 lck' \wedge \tilde{\mathbb{1}}^k lck' = \tilde{\mathbb{1}}^0 lck'))$ . But, then all the assumptions of Lemma 5.56 are fulfilled, and thus, it must be that:

$$\begin{aligned}
 \forall c @ \langle [\mathbb{T}, pc_{\mathbb{T}}, \mathbb{R}_{\mathbb{T}}, t_{\mathbb{T}}^a]_{\mathbb{T} \in \text{Thrd}}; \mathbb{x}, \mathbb{1} \rangle \in \mathbf{Conf} : \\
 (c^n \xrightarrow{\text{prg}} c \Rightarrow \exists \tilde{c} @ \langle [\mathbb{T}, pc_{\mathbb{T}}^{\tilde{c}}, \tilde{\mathbb{R}}_{\mathbb{T}}, \tilde{t}_{\mathbb{T}}^a]_{\mathbb{T} \in \text{Thrd}_{\tilde{c}}}; \tilde{\mathbb{x}}, \tilde{\mathbb{1}} \rangle \in \mathbf{Conf} : \\
 (\tilde{c}^k \xrightarrow{\text{prg}} \tilde{c} \wedge \\
 pc_{\mathbb{T}'} = pc_{\mathbb{T}'}^{\tilde{c}} \wedge \\
 \mathbb{R}_{\mathbb{T}'} \in \gamma_{\text{reg}}(\tilde{\mathbb{R}}_{\mathbb{T}'}) \wedge \\
 t_{\mathbb{T}'}^a \in \gamma_t(\tilde{t}_{\mathbb{T}'}) \wedge \\
 \exists \mathbb{x}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}) : (\forall x \in \mathbf{Var} : ((\mathbb{x} \ x) \mathbb{T}') \subseteq ((\mathbb{x}' \ x) \mathbb{T}')) \wedge \\
 \forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{1} \ lck) = \mathbb{T}' \Rightarrow \\
 (\text{STT}(\mathbb{1} \ lck) = \text{S}\check{\text{T}}\text{T}(\tilde{\mathbb{1}} \ lck) \wedge \\
 \text{OWN}(\mathbb{1} \ lck) = \text{O}\check{\text{W}}\text{N}(\tilde{\mathbb{1}} \ lck) \wedge \\
 \text{DL}(\mathbb{1} \ lck) \in \gamma_t(\check{\text{D}}\check{\text{L}}(\tilde{\mathbb{1}} \ lck)) \wedge \\
 \text{POWN}(\mathbb{1} \ lck) = \text{PO}\check{\text{W}}\text{N}(\tilde{\mathbb{1}} \ lck) \wedge \\
 \text{REL}(\mathbb{1} \ lck) \in \gamma_t(\check{\text{R}}\check{\text{E}}\check{\text{L}}(\tilde{\mathbb{1}} \ lck)) \wedge \\
 \min(\gamma_t(\check{\text{D}}\check{\text{L}}(\tilde{\mathbb{1}} \ lck)) = -\infty)))
 \end{aligned}$$

This concludes the proof of the base case.

Now consider the case that  $\mathbb{T}'$  must wait for  $j$  owner switches (i.e., `lock:s` and `unlock:s`) on  $lck'$  before it can acquire  $lck'$  itself; i.e.,  $\mathbb{T}'$  is owner number  $j+1$  among a set of competing threads to successfully acquire  $lck'$  (note that a thread could successfully acquire and release  $lck'$  several times while  $\mathbb{T}'$  is waiting to acquire  $lck'$ ; each time then counts as an owner switch). The induction assumption is that the lemma holds for all  $j$  owners that acquire  $lck'$  while  $\mathbb{T}'$  is waiting (i.e., frozen in the abstract case) and for all cases involving other locks.

Assume that  $\mathbb{T}'$  must wait for  $j$  owner switches on  $lck'$  before it successfully acquires  $lck'$  itself and that the lemma holds for all  $j$  owners that acquire  $lck'$  while  $\mathbb{T}'$  is waiting. Then it must be that  $\{n_1, n_2, \dots, n_m\} \neq \emptyset$ , and thus  $t_{\mathbb{T}'}^{a^0} \leq t_{\tilde{\mathbb{T}}'}^{a^0} = t_{\mathbb{T}'}^{a^0} + \text{TIME}(c^{n_1}, \mathbb{T}') + \text{TIME}(c^{n_2}, \mathbb{T}') + \dots + \text{TIME}(c^{n_m}, \mathbb{T}') =$

$t_{T'}^{a^{n_m}} + \text{TIME}(c^{n_m}, T')$  (c.f., Assumption 4.1 and Table 4.3).

Since the lemma holds for all  $j$  owners that acquire  $lck'$  while  $T'$  is waiting, and all other cases involving other locks, and  $\xrightarrow{\text{prg}}$  safely over-approximates the transitions described by  $\xrightarrow{\text{prg}}$  for all other cases (Lemma 5.56), including lock owner assignments (Lemma 5.55), it must be that there exists an abstract transition trace (starting at  $\tilde{c}^0$  and ending at  $\tilde{c}^k$ ) that safely represents the concrete trace from  $c^0$  to  $c^n$  for all  $j$  owners of  $lck'$ , at least until the point in which they release  $lck'$  and do not acquire it again (which is the important part of the trace to consider here), the order in which threads acquire  $lck'$  and all states, including the accumulated execution times (c.f., Lemmas 5.51 and 5.56 and the induction assumption). Thus, since  $T' \in \mathbf{Thrd}_{exe}^{c^{n_m}} \wedge \text{OWN}(\mathbb{1}^{n_m} lck') \neq T'$ ,  $\forall i \in \{n_m + 1, \dots, n - 1\} : T' \notin \mathbf{Thrd}_{exe}^{c^i}$  and  $T' \in \mathbf{Thrd}_{exe}^{c^n} \wedge \text{OWN}(\mathbb{1}^n lck') = \perp_{\text{thrd}} \wedge \text{OWN}(\mathbb{1}^{n'} lck') = T'$  (since it is assumed that  $T'$  acquires  $lck'$  in the transition from  $c^n$ ), it must be that  $lck'$  is released (by owner number  $j$ ) in a transition to  $c^{n'}$ , where  $c^{n_m} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^{n'} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n$  and  $n_m < n' \leq n$ . Thus, it must be that  $t_{T'}^{a^{n_m}} + \text{TIME}(c^{n_m}, T') = t_{T'}^{a^n} \leq \text{REL}(\mathbb{1}^n lck') \leq t_{T'}^{a^n} + \text{TIME}(c^n, T')$  (c.f., Assumption 4.1 and Table 4.3), where  $\text{REL}(\mathbb{1}^n lck') = \text{REL}(\mathbb{1}^{n'} lck')$  and  $\text{REL}(\mathbb{1}^n lck') \in \gamma_t(\text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{1}}^k lck'))$  (given the abstract trace from  $\tilde{c}^0$  to  $\tilde{c}^k$  that safely represents the trace from  $c^0$  to  $c^{n'}$  for the previous, i.e.,  $j^{\text{th}}$ , owner of  $lck'$ , it is easy to see that this is the result when the  $j^{\text{th}}$  owner issues `unlock`  $lck'$ ). But, then it is trivially the case that  $t_{T'}^{a^n} + \text{TIME}(c^n, T') \in \gamma_t(\text{DL}\text{LOCK}(\tilde{c}^k, lck'))$  (Lemma 5.53).

To show that `ACCTIME` is safe for this case, first note that  $T' \in \mathbf{Thrd}_{exe}^{\tilde{c}^k}$ ,  $\text{STM}(T', pc_{T'}^{\tilde{c}^k}) = [\text{lock } lck']^{pc_{T'}^{\tilde{c}^k}}$  and  $\text{S}\ddot{\text{T}}\text{T}(\tilde{\mathbb{1}}^{k''} lck') = \text{unlocked}$ . Also note that since  $t_{T'}^{a^n} + \text{TIME}(c^n, T') \in \gamma_t(\text{DL}\text{LOCK}(\tilde{c}^k, lck')) = \tilde{\text{D}}\text{L}(\tilde{\mathbb{1}}^{k''} lck')$ ,  $\text{DL}(\mathbb{1}^{n''} lck') = t_{T'}^{a^n} + \text{TIME}(c^n, T')$  (c.f., Tables 4.2 and 4.3 since  $T'$  acquires  $lck'$  in a transition from  $c^n$ ) and  $\min(\gamma_t(\tilde{t}_{T'}^{a^0} \dot{+}_t \text{ABSTIME}(\tilde{c}^0, T'))) \leq t_{T'}^{a^n} + \text{TIME}(c^n, T') \leq \max(\gamma_t(\tilde{\text{D}}\text{L}(\tilde{\mathbb{1}}^{k''} lck')))$  (c.f., Assumptions 4.1 and 5.50), it must be the case that  $\tilde{\text{D}}\text{L}(\tilde{\mathbb{1}}^{k''} lck') \not\lesssim_t \tilde{t}_{T'}^{a^0} \dot{+}_t \text{ABSTIME}(\tilde{c}^0, T')$ , which means that there are three branches of Algorithm 5.12 that must be considered here. Note that this also means that  $\text{DL}(\mathbb{1}^{n''} lck') \in \gamma_t(\tilde{\text{D}}\text{L}(\tilde{\mathbb{1}}^{k''} lck'))$ . For the sake of readability, let  $\tilde{c}^{k''} = \langle [T, pc_T^{\tilde{c}^k}, \tilde{\mathbb{1}}_T^k, \tilde{t}_T^{a^k}]_{T \in \mathbf{Thrd}_{ck}^{\tilde{c}^k}}, \tilde{x}^k, \tilde{\mathbb{1}}^{k''} \rangle$ . Also let  $\tilde{t}_{T'}^{a^l}$  be defined as  $\tilde{t}_T^{a^l}$  in Algorithm 5.12.

1. Since  $T'$  has been frozen while waiting to acquire  $lck'$ , it can be the case that  $\tilde{t}_{T'}^{a^k} \dot{+}_t \text{ABSTIME}(\tilde{c}^{k''}, T') \lesssim_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{1}}^{k''} lck')$ , where  $\tilde{t}_{T'}^{a^k} = \tilde{t}_T^{a^0}$ . (Note



that this does not necessarily have to be the case, though.) Let  $\tilde{c}'$  be any configuration derived before (i.e.,  $\tilde{c}' = \tilde{c}^{k''}$ ) or inside the **while**-loop.

First note that it cannot be that  $\text{ABSTIME}(\tilde{c}', T') = \alpha_t(\{0\})$  and  $\tilde{t}_{T'}^{a'} \dot{\vdash}_t \text{ABSTIME}(\tilde{c}', T') \dot{<}_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^{k''} lck')$  (c.f., Assumptions 4.3 and 5.50). This means that the **while**-loop will eventually terminate. It does so when  $\tilde{t}_{T'}^{a'}$  is the last point in time that safely represents the situation that  $T'$  has not yet acquired  $lck'$ ; thus, at  $\tilde{t}_{T'}^{a'} \dot{\vdash}_t \text{ABSTIME}(\tilde{c}', T')$ ,  $T'$  might have acquired  $lck'$  (i.e.,  $\tilde{t}_{T'}^{a'} \dot{<}_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^{k''} lck')$  and  $\tilde{t}_{T'}^{a'} \dot{\vdash}_t \text{ABSTIME}(\tilde{c}', T') \dot{\not\prec}_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^{k''} lck')$ ). In later references within this proof, the  $\tilde{t}_{T'}^{a'}$  obtained at the exit of the **while**-loop will be referred to as  $\tilde{t}_{T'}^{a^w}$ .

Since  $\tilde{t}_{T'}^{a^w} \dot{<}_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^{k''} lck')$  and  $\tilde{t}_{T'}^{a^w} \dot{\vdash}_t \text{ABSTIME}(\tilde{c}', T') \dot{\not\prec}_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^{k''} lck')$ , it is easy to see that this branch will lead to an auxiliary configuration,  $\tilde{c}^{k'}$ , such that  $\tilde{c}^k \xrightarrow{\text{prg}} \tilde{c}^{k'}$ , for which  $\tilde{\mathbb{I}}^{k'} lck' = \tilde{\mathbb{I}}^{k''} lck'$ ; i.e.,  $T'$  has not yet acquired  $lck'$ . The only difference for  $T'$  between  $\tilde{c}^k$  and  $\tilde{c}^{k'}$  is that, in the latter, it has an advanced accumulated execution time (c.f., Table 5.5). Since  $\tilde{t}_{T'}^{a^w} \dot{\vdash}_t \text{ABSTIME}(\tilde{c}', T') \dot{\not\prec}_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^{k''} lck')$ , it is also easy to see that this branch of Algorithm 5.12 will not be taken when  $\text{ACCTIME}$  is called based on  $\tilde{c}^{k'}$ . Note that it must be that  $|\{n_1, n_2, \dots, n_m\}|$  is greater than or equal to the number of iterations of the **while**-loop (Assumption 5.50 and Lemma 5.52). Thus, it is also easy to see that  $\text{D}\ddot{\text{L}}(\tilde{\mathbb{I}}^{k''} lck') \dot{\not\prec}_t \tilde{t}_{T'}^{a^w} \dot{\vdash}_t \text{ABSTIME}(\tilde{c}^{k'}, T')$  since  $\text{TIME}(c^i, T') \in \gamma_t(\text{ABSTIME}(\tilde{c}^{k'}, T'))$ , where  $i \in \{n_1, n_2, \dots, n_m\}$  is the corresponding concrete configuration for which the **while**-loop terminates (Assumption 5.50). This means that for  $\tilde{c}^{k'}$ , one of the two last branches (considered in the next two bullets) of Algorithm 5.12 will apply.

2. First note that it must be that  $\text{PO}\ddot{\text{W}}\text{N}(\tilde{\mathbb{I}}^{k''} lck') \neq T'$  since  $T'$  has been waiting for at least one other thread to release  $lck'$  before it is allowed to acquire it (c.f., Tables 5.5 and 5.6 and the induction assumption). If, on the other hand,  $\text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^{k''} lck') \dot{<}_t \tilde{t}_{T'}^{a'} \dot{\vdash}_t \text{ABSTIME}(\tilde{c}^{k''}, T')$ , then the proof is equivalent to the corresponding part of the proof for Lemma 5.54 since  $t_{T'}^{a''} + \text{TIME}(c^n, T') = \text{D}\ddot{\text{L}}(\mathbb{I}^{n''} lck')$ ,  $\text{D}\ddot{\text{L}}(\mathbb{I}^{n''} lck') \in \gamma_t(\text{D}\ddot{\text{L}}(\tilde{\mathbb{I}}^{k''} lck'))$  and  $\text{R}\ddot{\text{E}}\text{L}(\mathbb{I}^{n''} lck') \in \gamma_t(\text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^{k''} lck'))$ . Note that this also applies if  $\tilde{t}_{T'}^{a'} = \tilde{t}_{T'}^{a^w}$  (i.e., if  $\tilde{c}^{k''} = \tilde{c}^{k'}$ ) since it must be that  $t_{T'}^{a''} \in \gamma_t(\tilde{t}_{T'}^{a^w})$ , which follows from Assumption 5.50 and Lemma 5.51 based on 1 above.
3. If  $(\tilde{t}_{T'}^{a'} \dot{\vdash}_t \text{ABSTIME}(\tilde{c}', T')) \dot{\cap}_t \text{R}\ddot{\text{E}}\text{L}(\tilde{\mathbb{I}}^{k''} lck') \neq \dot{\perp}_t$ , then let  $\tilde{t}_{T'}^{a''} = \tilde{t}_{T'}^{a'} \dot{\vdash}_t$

$\text{ABSTIME}(\tilde{c}', T)$  (where  $\tilde{t}'_{T'}$  is thus defined as in Algorithm 5.12 and  $\tilde{t}'_{T'}$  is either  $\tilde{t}'_{T'}^k$  or  $\tilde{t}'_{T'}^w$  and  $\tilde{c}'$  is either  $\tilde{c}^{k''}$  or  $\tilde{c}^{k'}$ ), which is obviously a safe estimation of the first point in time when  $T'$  can acquire  $lck'$ .

Now, let  $\tilde{c}'$  be any configuration derived before (i.e.,  $\tilde{c}' = \tilde{c}^{k''}$  or  $\tilde{c}' = \tilde{c}^{k'}$ ) or inside the **repeat**-loop (and the corresponding for  $\tilde{t}'_{T'}$ ), which will now be considered. Note that  $\tilde{t}'_{T'} = \tilde{t}_T$  is used to exit the loop in case  $\tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck') \prec_t \tilde{t}'_{T'} \tilde{t}_T \text{ABSTIME}(\tilde{c}', T')$  or  $0 \in \gamma_t(\text{ABSTIME}(\tilde{c}', T'))$ , where the latter case means that a  $\tilde{t}'_{T'}$  such that  $\text{R}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{I}}^{k''} lck') \prec_t \tilde{t}'_{T'}$  cannot be derived (c.f., Assumption 5.50).

- (a) If  $\tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck') \prec_t \tilde{t}'_{T'} \tilde{t}_T \text{ABSTIME}(\tilde{c}', T')$ , then it must be that  $\tilde{t}'_{T'}$  is a safe estimation of the last point in time when  $T'$  can acquire  $lck'$  since  $t_{T'}^n + \text{TIME}(c^n, T') = \text{DL}(\mathbb{I}^{n''} lck')$ ,  $\text{DL}(\mathbb{I}^{n''} lck') \in \gamma_t(\tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck'))$  and  $T'$  acquires  $lck'$  in a transition from  $c^n$  (c.f., Assumption 5.50 and Lemma 5.52 which means that the total number of iterations of the **repeat**-loop, and possibly the **while**-loop from 1, must be greater than or equal to  $|\{n_1, n_2, \dots, n_m, n\}|$ ). Thus, it must be that  $t_{T'}^n + \text{TIME}(c^n, T') \in \gamma_t((\tilde{t}'_{T'} \sqcup_t \tilde{t}'_{T'}) \tilde{t}_T \tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck') \tilde{t}_T (\text{R}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{I}}^{k''} lck') \sqcup_t \alpha_t(\{\infty\})))$  since  $\text{REL}(\mathbb{I}^{n''} lck') \in \gamma_t(\text{R}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{I}}^{k''} lck'))$  and  $\min(\gamma_t(\tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck'))) = -\infty$ .
- (b) If  $0 \in \gamma_t(\text{ABSTIME}(\tilde{c}', T'))$ , then it must obviously be that  $\tilde{t} \tilde{t}_T \text{ABSTIME}(\tilde{c}'', T')$ , where  $\tilde{t} = (\tilde{t}'_{T'} \sqcup_t \alpha_t(\{\infty\})) \tilde{t}_T \text{R}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{I}}^{k''} lck')$ , and  $\tilde{c}'' = \langle [T, pc_T^{c^k}, \tilde{\mathbb{I}}_T^k, (T = T' ? \tilde{t} : \tilde{t}'_{T'}^k)]_{T \in \text{Thrd}_{c^k}}, \tilde{x}^k, \tilde{\mathbb{I}}^{k''} \rangle$ , is a safe approximation of the last point in time when  $T'$  can (or rather, will) acquire  $lck'$  (c.f., Assumption 5.50 and Lemma 5.52). Thus, it must be that  $t_{T'}^n + \text{TIME}(c^n, T') \in \gamma_t((\tilde{t}'_{T'} \sqcup_t \tilde{t}'_{T'}) \tilde{t}_T \tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck') \tilde{t}_T (\text{R}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{I}}^{k''} lck') \sqcup_t \alpha_t(\{\infty\})))$  since  $\text{REL}(\mathbb{I}^{n''} lck') \in \gamma_t(\text{R}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{I}}^{k''} lck'))$ ,  $\text{DL}(\mathbb{I}^{n''} lck') \in \gamma_t(\tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck'))$ ,  $t_{T'}^n + \text{TIME}(c^n, T') = \text{DL}(\mathbb{I}^{n''} lck')$ ,  $\min(\gamma_t(\tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck'))) = -\infty$  and  $T'$  acquires  $lck'$  in a transition from  $c^n$ .
- (c) If  $0 \notin \gamma_t(\text{ABSTIME}(\tilde{c}', T'))$  and also  $\tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck') \prec_t \tilde{t}'_{T'} \tilde{t}_T \text{ABSTIME}(\tilde{c}', T')$ , then it must be that, at the end of some iteration of the **repeat**-loop,  $\text{R}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{I}}^{k''} lck') \prec_t \tilde{t}'_{T'}$ . For such a  $\tilde{t}'_{T'}$ , it is easy to see that  $t_{T'}^n + \text{TIME}(c^n, T') \in \gamma_t((\tilde{t}'_{T'} \sqcup_t \tilde{t}'_{T'}) \tilde{t}_T \tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck') \tilde{t}_T (\text{R}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{I}}^{k''} lck') \sqcup_t \alpha_t(\{\infty\})))$  since  $\text{REL}(\mathbb{I}^{n''} lck') \in \gamma_t(\text{R}\tilde{\text{E}}\tilde{\text{L}}(\tilde{\mathbb{I}}^{k''} lck'))$ ,  $\text{DL}(\mathbb{I}^{n''} lck') \in \gamma_t(\tilde{D}\tilde{L}(\tilde{\mathbb{I}}^{k''} lck'))$ ,  $t_{T'}^n +$

$\text{TIME}(c^n, T') = \text{DL}(\mathbb{1}^{n''} lck')$ ,  $\min(\gamma_t(\text{DL}(\tilde{\mathbb{1}}^{k''} lck')))) = -\infty$  and  $T'$  acquires  $lck'$  in a transition from  $c^n$  (c.f., Assumption 5.50 and Lemma 5.52 which means that the total number of iterations of the **repeat**-loop, and possibly the **while**-loop from 1, must be greater than or equal to  $|\{n_1, n_2, \dots, n_m, n\}|$ ).

Thus, it has been shown that  $t_{T'}^{a^n} + \text{TIME}(c^n, T') \in \gamma_t(\text{ACCTIME}(\tilde{c}' @ \langle [T, pc'_T, \tilde{x}'_T, \tilde{t}'_T]_{T \in \text{Thrd}_{\tilde{c}^k}}, \tilde{x}', \tilde{\mathbb{1}}' \rangle, \text{Thrd}_{\tilde{c}'_{exe}}, T')$ ), for both the case that  $\tilde{c}'$  is  $\tilde{c}^{k''}$  (if  $\tilde{t}'_T^{a^k} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^{k''}, T') \tilde{\prec}_t \text{REL}(\tilde{\mathbb{1}}^{k''} lck')$ ) and  $\tilde{c}'$  is  $\tilde{c}^{k'}$  (if  $\tilde{t}'_T^{a^k} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^{k''}, T') \tilde{\prec}_t \text{REL}(\tilde{\mathbb{1}}^{k''} lck')$ ), where  $\tilde{c}^{k''}$  and  $\tilde{c}^{k'}$  are as defined above. If  $\tilde{t}'_T^{a^k} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^{k''}, T') \tilde{\prec}_t \text{REL}(\tilde{\mathbb{1}}^{k''} lck')$ , it is easy to see that

$$\begin{aligned}
 pc_{T'}^n &= pc_{T'}^{\tilde{c}^{k'}}, \\
 \mathbb{1}_{T'}^n &\in \gamma_{\text{reg}}(\tilde{\mathbb{1}}_{T'}^{k'}), \\
 \exists \tilde{x}' \in \gamma_{\text{var}}(\tilde{x}'^{k'}) &: (\forall x \in \mathbf{Var} : ((\mathbb{x}^n x) T') \subseteq ((\tilde{x}' x) T')) \text{ and} \\
 \forall lck \in \mathbf{Lck} &: (\text{OWN}(\mathbb{1}^n lck) = T' \Rightarrow (\text{STT}(\mathbb{1}^n lck) = \text{s}\tilde{\text{T}}\text{T}(\tilde{\mathbb{1}}^{k'} lck) \wedge \\
 &\quad \text{OWN}(\mathbb{1}^n lck) = \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^{k'} lck) \wedge \\
 &\quad \text{DL}(\mathbb{1}^n lck) \in \gamma_t(\text{DL}(\tilde{\mathbb{1}}^{k'} lck)) \wedge \\
 &\quad \text{POWN}(\mathbb{1}^n lck) = \text{PO}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}}^{k'} lck) \wedge \\
 &\quad \text{REL}(\mathbb{1}^n lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{1}}^{k'} lck)) \wedge \\
 &\quad \min(\gamma_t(\text{DL}(\tilde{\mathbb{1}}^{k'} lck))) = -\infty))
 \end{aligned}$$

since, for  $T'$ , the accumulated execution time is the only state affected by the transition  $\tilde{c}^k \xrightarrow{\text{prg}} \tilde{c}^{k'}$  (c.f., Table 5.5; this means that, e.g.,  $\tilde{\mathbb{1}}^{k'} lck' = \tilde{\mathbb{1}}^{k''} lck'$ ) and TRIM is safe (Lemma 5.27). Thus, for both transition sequences described by  $\tilde{c}^k \xrightarrow{\text{prg}} \tilde{c}^{k'} \xrightarrow{\text{prg}} \tilde{c}$  and  $\tilde{c}^k \xrightarrow{\text{prg}} \tilde{c}$ , where  $\tilde{c} @ \langle [T, pc_{T'}^{\tilde{c}}, \tilde{x}_T, \tilde{t}_T^a]_{T \in \text{Thrd}_{\tilde{c}^k}}, \tilde{x}, \tilde{\mathbb{1}} \rangle \in \mathbf{Conf}$ , for the two different cases  $(\tilde{t}'_T^{a^k} \tilde{\vdash}_t \text{ABSTIME}(\tilde{c}^{k''}, T') \tilde{\prec}_t \text{REL}(\tilde{\mathbb{1}}^{k''} lck'))$  and  $\tilde{t}'_T^{a^k} \tilde{\vdash}_t$

ABSTIME( $\tilde{c}^{k''}, T'$ )  $\not\prec_t$   $\text{REL}(\tilde{\mathbb{I}}^{k''} lck')$ , respectively), it must be that

$$\begin{aligned}
 pc_{T'} &= pc_{T'}^{\tilde{c}}, \\
 \mathbb{r}_{T'} &\in \gamma_{\text{reg}}(\tilde{\mathbb{r}}_{T'}), \\
 t_{T'}^a &\in \gamma_t(\tilde{t}_{T'}^a), \\
 \exists \mathbb{x}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}) : (\forall x \in \mathbf{Var} : ((\mathbb{x} \ x) T') \subseteq ((\mathbb{x}' \ x) T')) \text{ and} \\
 \forall lck \in \mathbf{Lck} : (\text{OWN}(\mathbb{I} lck) = T' \Rightarrow & (\text{STT}(\mathbb{I} lck) = \text{STT}(\tilde{\mathbb{I}} lck) \wedge \\
 & \text{OWN}(\mathbb{I} lck) = \text{OWN}(\tilde{\mathbb{I}} lck) \wedge \\
 & \text{DL}(\mathbb{I} lck) \in \gamma_t(\text{DL}(\tilde{\mathbb{I}} lck)) \wedge \\
 & \text{POWN}(\mathbb{I} lck) = \text{POWN}(\tilde{\mathbb{I}} lck) \wedge \\
 & \text{REL}(\mathbb{I} lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}} lck)) \wedge \\
 & \min(\gamma_t(\text{DL}(\tilde{\mathbb{I}} lck))) = -\infty))
 \end{aligned}$$

where  $c^n \xrightarrow{\text{prg}} c$  for some  $c @ \langle [T, pc_T, \mathbb{r}_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}, \mathbb{I} \rangle \in \mathbf{Conf}$ , since  $\xrightarrow{\text{ax}}$  is a safe approximation of  $\xrightarrow{\text{ax}}$  (Lemma 5.49),  $\text{DL}(\mathbb{I} lck') = t_{T'}^a + \text{TIME}(c^n, T')$  (Table 4.2) and **TRIM** is safe (Lemma 5.27). But then the lemma holds.  $\blacksquare$

Lemma 5.58 shows that  $\xrightarrow{\text{prg}}$  can be used to safely approximate any finite concrete transition sequence. Note that the approximation is safe if either no thread issues a `load`-statement on a global variable or that the thread issuing the `load`-statement is the sole thread in  $\mathbf{Thrd}_{\text{exe}}$  in any step of the transition sequence.

**Lemma 5.58 (Soundness of  $\xrightarrow{\text{prg}}$ , final state):**

Given the valid concrete configurations (c.f., Definition 4.4)  $c^0 @ \langle [T, pc_T^0, \mathbb{r}_T^0, t_T^{a^0}]_{T \in \mathbf{Thrd}_e}, \mathbb{x}^0, \mathbb{I}^0 \rangle \in \mathbf{Conf}$  and  $c^n @ \langle [T, pc_T^n, \mathbb{r}_T^n, t_T^{a^n}]_{T \in \mathbf{Thrd}_e}, \mathbb{x}^n, \mathbb{I}^n \rangle \in \mathbf{Conf}$  and the abstract configuration  $\tilde{c}^0 @ \langle [T, pc_T^{\tilde{c}^0}, \tilde{\mathbb{r}}_T^0, \tilde{t}_T^{a^0}]_{T \in \mathbf{Thrd}_e}, \tilde{\mathbb{x}}^0, \tilde{\mathbb{I}}^0 \rangle \in \mathbf{Conf}$ , such that  $c^0 \in \gamma_{\text{conf}}(\tilde{c}^0)$ ,  $\forall lck \in \mathbf{Lck} : \min(\gamma_t(\text{DL}(\tilde{\mathbb{I}}^0 lck))) =$

$$\begin{aligned}
 & -\infty, 0 < n \text{ and } c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n, \xrightarrow{\sim} \text{ satisfies} \\
 & (\forall T \in \mathbf{Thrd}_{\varepsilon} : \text{STM}(T, pc_T^n) = [\text{halt}]^{pc_T^n}) \\
 & \Rightarrow \\
 & (\exists \tilde{c}^k @ \langle [T, pc_T^k, \tilde{\mathbb{I}}_T^k, \tilde{t}_T^k]_{T \in \mathbf{Thrd}_{\varepsilon}}, \tilde{\mathbb{X}}^k, \tilde{\mathbb{I}}^k \rangle \in \mathbf{C\o n f} : \\
 & \quad (\tilde{c}^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^k \wedge \\
 & \quad (\forall i \in \{0, \dots, k-1\} : (|\mathbf{Thrd}_{exe}^i| \not\geq 1 \vee \\
 & \quad \quad \{T \in \mathbf{Thrd}_{exe}^i \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_{\mathbf{g}} : \\
 & \quad \quad \quad \text{STM}(T, pc_T^i) = [\text{load } r \text{ from } x]^{pc_T^i}\} = \emptyset)) \\
 & \Rightarrow \\
 & (\forall T \in \mathbf{Thrd}_{\varepsilon} : (pc_T^n = pc_T^k \wedge \\
 & \quad \mathbb{I}_T^n \in \gamma_{reg}(\tilde{\mathbb{I}}_T^k) \wedge \\
 & \quad t_T^{a^n} \in \gamma_t(\tilde{t}_T^{a^k}) \wedge \\
 & \quad \exists \mathbb{X}' \in \gamma_{var}(\tilde{\mathbb{X}}^k) : (\forall x \in \mathbf{Var} : ((\mathbb{X}^n x) T) \subseteq ((\mathbb{X}' x) T))) \wedge \\
 & \quad \forall lck \in \mathbf{Lck} : (\text{STT}(\mathbb{I}^n lck) = \text{STT}(\tilde{\mathbb{I}}^k lck) \wedge \\
 & \quad \text{OWN}(\mathbb{I}^n lck) = \text{OWN}(\tilde{\mathbb{I}}^k lck) \wedge \\
 & \quad \text{DL}(\mathbb{I}^n lck) \in \gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^k lck)) \wedge \\
 & \quad \text{POWN}(\mathbb{I}^n lck) = \text{POWN}(\tilde{\mathbb{I}}^k lck) \wedge \\
 & \quad \text{REL}(\mathbb{I}^n lck) \in \gamma_t(\tilde{\text{REL}}(\tilde{\mathbb{I}}^k lck)) \wedge \\
 & \quad \min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^k lck))) = -\infty)))
 \end{aligned}$$

where, for all  $i \in \{0, \dots, k-1\}$ ,  $\mathbf{Thrd}_{exe}^i$  is as defined in Table 5.6, and  $\mathbf{Var}_{\mathbf{g}}$  contains all  $x \in \mathbf{Var}$  such that  $x$  can be written to by one thread and read from by another thread (i.e., there might be a data dependency between the threads; note that  $\mathbf{Var}_{\mathbf{g}}$  can be derived using Algorithm 6.9).  $\square$

PROOF. Assume that the valid (c.f., Definition 4.4) concrete configurations  $c^0 @ \langle [T, pc_T^0, \mathbb{I}_T^0, t_T^{a^0}]_{T \in \mathbf{Thrd}_{\varepsilon}}, \mathbb{X}^0, \mathbb{I}^0 \rangle \in \mathbf{C\o n f}$  and  $c^n @ \langle [T, pc_T^n, \mathbb{I}_T^n, t_T^{a^n}]_{T \in \mathbf{Thrd}_{\varepsilon}}, \mathbb{X}^n, \mathbb{I}^n \rangle \in \mathbf{C\o n f}$  and the abstract configuration  $\tilde{c}^0 @ \langle [T, pc_T^{\tilde{c}^0}, \tilde{\mathbb{I}}_T^0, \tilde{t}_T^{a^0}]_{T \in \mathbf{Thrd}_{\varepsilon}}, \tilde{\mathbb{X}}^0, \tilde{\mathbb{I}}^0 \rangle \in \mathbf{C\o n f}$  are such that  $c^0 \in \gamma_{conf}(\tilde{c}^0)$ ,  $c^0 \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^n$ ,  $\forall lck \in \mathbf{Lck} : \min(\gamma_t(\tilde{\text{DL}}(\tilde{\mathbb{I}}^0 lck))) = -\infty$  and  $\forall T \in \mathbf{Thrd}_{\varepsilon} : \text{STM}(T, pc_T^n) = [\text{halt}]^{pc_T^n}$ .

Note that since  $\forall T \in \mathbf{Thrd}_{\varepsilon} : \text{STM}(T, pc_T^n) = [\text{halt}]^{pc_T^n}$ , it must be that all threads trying to acquire a lock at some point will eventually successfully do so (i.e., there are no deadlocks etc.) and there are no infinite loops. Also note that the possible abstract combinations of the owner and the state for some lock,  $lck \in \mathbf{Lck}$ , given a reference thread,  $T \in \mathbf{Thrd}_{\varepsilon}$ , in a lock state,  $\tilde{\mathbb{I}}$ , resulting from a transition using  $\xrightarrow{\text{prg}}$  are by definition as follows.

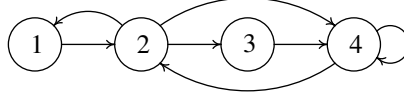


Figure 5.7: Abstract lock state transitions.

1.  $\text{OWN}(\tilde{l}ck) \notin \{\perp_{thrd}, T\}$  – This means that  $T$  will be frozen if it issues `lock lck` and occurs when  $\text{OWN}(lck) \neq T$ .
2.  $\text{OWN}(\tilde{l}ck) = \perp_{thrd}$  – This occurs when  $\text{OWN}(lck) = \perp_{thrd}$ . A safe (over-approximate) owner assignment will occur if  $T$  issues `lock lck`. (The soundness is given by that it is trivially the case that for all concrete and abstract configurations consisting of the threads in  $\mathbf{Thrd}_{\tilde{c}}$ ,  $\{T' \in \mathbf{Thrd}_{exe} \mid \text{STM}(T', pc_{T'}) = [\text{lock } lck]^{pc_{T'}}\} \subseteq \{T' \in \mathbf{Thrd}_{\tilde{c}} \mid \exists l \in \mathbf{Lbl}_{T'} : \text{STM}(T', l) = [\text{lock } lck]^l\}$ ; c.f., Table 4.3.)
3.  $\text{OWN}(\tilde{l}ck) = T \wedge \tilde{\text{ST}}T(\tilde{l}ck) = \text{unlocked}$  – This means that  $T$  has not yet done `lock lck`, but some other thread has (with the result that  $T$  was assigned `lck`; c.f., the discussion for state 2). If  $T$  issues `lock lck` within the deadline, it will successfully acquire `lck`. If it does not, there is no corresponding concrete situation described by the owner assignment, given that  $\text{DL}(lck) \in \tilde{\text{DL}}(\tilde{l}ck)$ , and thus, the configuration will be discontinued; c.f., Algorithms 6.1 and 6.6, which are discussed in Chapter 6. This occurs when  $\text{OWN}(lck) = \perp_{thrd}$ .
4.  $\text{OWN}(\tilde{l}ck) = T \wedge \tilde{\text{ST}}T(\tilde{l}ck) = \text{locked}$  – This occurs when  $\text{OWN}(lck) = T$ .

The possible transitions between these abstract states (as defined by  $\xrightarrow[\text{prg}]{\text{ax}}$  and  $\xrightarrow[\text{prg}]{\text{ax}}$ ) are depicted in Figure 5.7. State 3 (a result from the over-approximate owner assignment performed by  $\xrightarrow[\text{prg}]{\text{ax}}$ ) is needed because  $\mathbf{Time} = \mathbf{Intv}$ , which means that even if a thread acquires a lock first in the abstract case, it could be that some other thread could actually acquire the lock first in the corresponding concrete case. Lemma 5.55 gives that  $\xrightarrow[\text{prg}]{\text{ax}}$  covers all the possible concrete situations for lock owner assignments, regardless of which thread issues `lock lck` first in the abstract case; c.f., a transition from state 2 to state 4, possibly via state 3.

This proof will partly be conducted using induction on how the states of a configuration are changed during transitions, based on one thread at

a time. Therefore, consider  $c^f @ \langle [T, pc_T^f, \mathbb{I}_T^f, t_T^{a^f}]_{T \in \mathbf{Thrd}_{\bar{c}}}, \mathbb{X}^f, \mathbb{I}^f \rangle \in \mathbf{Conf}$ ,  $c^g @ \langle [T, pc_T^g, \mathbb{I}_T^g, t_T^{a^g}]_{T \in \mathbf{Thrd}_{\bar{c}}}, \mathbb{X}^g, \mathbb{I}^g \rangle \in \mathbf{Conf}$ ,  $\tilde{c}^i @ \langle [T, pc_T^{\tilde{c}^i}, \tilde{\mathbb{I}}_T^i, \tilde{t}_T^{a^i}]_{T \in \mathbf{Thrd}_{\bar{c}}}, \tilde{\mathbb{X}}^i, \tilde{\mathbb{I}}^i \rangle \in \mathbf{Conf}$  and  $T' \in \mathbf{Thrd}_{\bar{c}}$  such that

$$\begin{aligned}
 & c^f \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c^g \wedge \\
 & 0 \leq f < g \leq n \wedge \\
 & \forall h \in \{f, \dots, g-2\} : (T' \notin \mathbf{Thrd}_{exe}^{c^h} \vee \\
 & \quad \exists lck \in \mathbf{Lck} : (\text{STM}(T', pc_{T'}^h) = [\text{lock } lck]^{pc_{T'}^h} \wedge \\
 & \quad \quad \text{OWN}(\mathbb{I}^{h+1} lck) \neq T')) \wedge \\
 & T' \in \mathbf{Thrd}_{exe}^{c^{g-1}} \wedge \\
 & \forall lck \in \mathbf{Lck} : \text{STM}(T', pc_{T'}^{g-1}) = [\text{lock } lck]^{pc_{T'}^{g-1}} \Rightarrow \text{OWN}(\mathbb{I}^g lck) = T' \wedge \\
 & pc_{T'}^f = pc_{T'}^{\tilde{c}^i} \wedge \\
 & \mathbb{I}_{T'}^f \in \gamma_{reg}(\tilde{\mathbb{I}}_{T'}^i) \wedge \\
 & t_{T'}^{a^f} \in \gamma_t(\tilde{t}_{T'}^{a^i}) \wedge \\
 & \exists \mathbb{X}' \in \gamma_{var}(\tilde{\mathbb{X}}^i) : \forall x \in \mathbf{Var} : \forall T \in \mathbf{Thrd} : ((\mathbb{X}^f x) T) \subseteq ((\mathbb{X}' x) T) \wedge \\
 & \forall lck \in \mathbf{Lck} : ((\text{OWN}(\mathbb{I}^f lck) \neq \perp_{thrd} \Rightarrow (\text{STT}(\mathbb{I}^f lck) = \text{STT}(\tilde{\mathbb{I}}^i lck) \wedge \\
 & \quad \text{OWN}(\mathbb{I}^f lck) = \text{OWN}(\tilde{\mathbb{I}}^i lck) \wedge \\
 & \quad \text{DL}(\mathbb{I}^f lck) \in \gamma_t(\text{DL}(\tilde{\mathbb{I}}^i lck)) \wedge \\
 & \quad \text{POWN}(\mathbb{I}^f lck) = \text{POWN}(\tilde{\mathbb{I}}^i lck) \wedge \\
 & \quad \text{REL}(\mathbb{I}^f lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}^i lck)) \wedge \\
 & \quad \min(\gamma_t(\text{DL}(\tilde{\mathbb{I}}^i lck))) = -\infty)) \wedge \\
 & (\text{OWN}(\mathbb{I}^f lck) = \perp_{thrd} \Rightarrow ((\text{OWN}(\mathbb{I}^f lck) = \text{OWN}(\tilde{\mathbb{I}}^i lck) \vee \\
 & \quad (\text{OWN}(\tilde{\mathbb{I}}^i lck) = T' \wedge \\
 & \quad \text{STT}(\tilde{\mathbb{I}}^i lck) = \text{unlocked} \wedge \\
 & \quad t_{T'}^{a^g} \in \gamma_t(\text{DL}(\tilde{\mathbb{I}}^i lck)) \wedge \\
 & \quad \min(\gamma_t(\text{DL}(\tilde{\mathbb{I}}^i lck))) = -\infty)) \wedge \\
 & \quad \text{POWN}(\mathbb{I}^f lck) = \text{POWN}(\tilde{\mathbb{I}}^i lck) \wedge \\
 & \quad \text{REL}(\mathbb{I}^f lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}^i lck)))))) \wedge \\
 & \forall h \in \{f, \dots, g-1\} : (|\mathbf{Thrd}_{exe}^{c^h}| \neq 1 \vee \\
 & \quad \{T \in \mathbf{Thrd}_{exe}^{c^h} \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : \\
 & \quad \quad \text{STM}(T, pc_T^{c^h}) = [\text{load } r \text{ from } x]^{pc_T^{c^h}}\} = \emptyset)
 \end{aligned}$$

where  $\mathbf{Thrd}_{exe}$  is as defined in Table 4.3. This is the induction assumption. Then it is easy to see that there exists a  $\tilde{c}^j @ \langle [T, pc_T^{\tilde{c}^j}, \tilde{\mathbb{I}}_T^j, \tilde{t}_T^{a^j}]_{T \in \mathbf{Thrd}_{\bar{c}}}, \tilde{\mathbb{X}}^j, \tilde{\mathbb{I}}^j \rangle \in$

**Cōnf**, such that

$$\begin{aligned}
& \tilde{c}^i \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}^j \wedge \\
& pc_{T'}^g = pc_{T'}^{\tilde{c}^j} \wedge \\
& r_{T'}^g \in \gamma_{\text{reg}}(\tilde{r}_{T'}^j) \wedge \\
& t_{T'}^{a^g} \in \gamma_t(\tilde{t}_{T'}^{a^j}) \wedge \\
& \exists \mathbb{x}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}^j) : (\forall x \in \mathbf{Var} : ((\mathbb{x}^g x) T') \subseteq ((\mathbb{x}' x) T')) \wedge \\
& \forall lck \in \mathbf{Lck} : ((\text{OWN}(\mathbb{I}^j lck) = T' \vee \\
& \quad \text{OWN}(\mathbb{I}^g lck) = T') \Rightarrow (\text{STT}(\mathbb{I}^g lck) = \text{STT}(\tilde{\mathbb{I}}^j lck) \wedge \\
& \quad \text{OWN}(\mathbb{I}^g lck) = \text{OWN}(\tilde{\mathbb{I}}^j lck) \wedge \\
& \quad \text{DL}(\mathbb{I}^g lck) \in \gamma_t(\text{DL}(\tilde{\mathbb{I}}^j lck)) \wedge \\
& \quad \text{POWN}(\mathbb{I}^g lck) = \text{POWN}(\tilde{\mathbb{I}}^j lck) \wedge \\
& \quad \text{REL}(\mathbb{I}^g lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}^j lck)) \wedge \\
& \quad \min(\gamma_t(\text{DL}(\tilde{\mathbb{I}}^j lck))) = -\infty))
\end{aligned}$$

(Lemmas 5.55, 5.56 and 5.57). Note that even if for some lock,  $lck \in \mathbf{Lck}$ ,  $T'$  issues `lock lck` but  $lck$  is assigned to some other thread,  $T'$  will eventually be assigned  $lck$  so that it can acquire it (since all threads that want to acquire a lock eventually will be able to do so). For such cases,  $T'$  is the owner of  $lck$  in  $c^g$  and  $\tilde{c}^j$  (c.f., Lemmas 5.56 and 5.57).

Now consider the base case for the induction part of the proof. Since  $c^0 \in \gamma_{\text{conf}}(\tilde{c}^0)$ ,  $\forall lck \in \mathbf{Lck} : \min(\gamma_t(\text{DL}(\tilde{\mathbb{I}}^0 lck))) = -\infty$  and  $c^0$  is valid, it is easy to see that

$$\begin{aligned}
& \forall T \in \mathbf{Thrd}_{\tilde{c}} : (pc_T^0 = pc_T^{\tilde{c}^0} \wedge \\
& \quad r_T^0 \in \gamma_{\text{reg}}(\tilde{r}_T^0) \wedge \\
& \quad t_T^{a^0} \in \gamma_t(\tilde{t}_T^{a^0}) \wedge \\
& \quad \exists \mathbb{x}' \in \gamma_{\text{var}}(\tilde{\mathbb{x}}^0) : \forall x \in \mathbf{Var} : ((\mathbb{x}^0 x) T) \subseteq ((\mathbb{x}' x) T)) \wedge \\
& \forall lck \in \mathbf{Lck} : (\text{STT}(\mathbb{I}^0 lck) = \text{STT}(\tilde{\mathbb{I}}^0 lck) \wedge \\
& \quad \text{OWN}(\mathbb{I}^0 lck) = \text{OWN}(\tilde{\mathbb{I}}^0 lck) \wedge \\
& \quad \text{DL}(\mathbb{I}^0 lck) \in \gamma_t(\text{DL}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
& \quad \text{POWN}(\mathbb{I}^0 lck) = \text{POWN}(\tilde{\mathbb{I}}^0 lck) \wedge \\
& \quad \text{REL}(\mathbb{I}^0 lck) \in \gamma_t(\text{REL}(\tilde{\mathbb{I}}^0 lck)) \wedge \\
& \quad \min(\gamma_t(\text{DL}(\tilde{\mathbb{I}}^0 lck))) = -\infty)
\end{aligned}$$

which means that as long as  $\forall h \in \{0, \dots, k-1\} : (|\mathbf{Thrd}_{\text{exe}}^{c^h}| \not\geq 1 \vee \{T \in \mathbf{Thrd}_{\text{exe}}^{c^h} \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : \text{STM}(T, pc_T^{c^h}) = [\text{load } r \text{ from } x]^{pc_T^{c^h}}\} = \emptyset)$ , the induction holds for all threads in  $\mathbf{Thrd}_{\tilde{c}}$ .



Note that by definition,  $\mathbb{1}^n lck = \mathbb{1}^0 lck$  (c.f., Tables 4.2 and 4.3) and  $\tilde{\mathbb{1}}^k lck = \tilde{\mathbb{1}}^0 lck$  (c.f., Tables 5.5 and 5.6) if  $lck$  is never acquired by any thread, or never released by its initially owning thread (i.e., the owner of  $lck$  in  $c^0$  and  $\tilde{c}^0$ , respectively).

This concludes the proof. ■

Because of the unsafe nature of  $\xrightarrow{prg}$  (i.e., it cannot safely approximate all concrete transition sequences), it cannot be directly used to derive a safe set of possible final configurations (i.e., configurations such that all threads are issuing `halt`). It must instead be encapsulated by an algorithm that uses it in a safe manner and handles the unsafe situations explicitly. Such an algorithm is defined in the next chapter.



## Chapter 6

# Safe Timing Analysis by Abstract Execution

In this chapter, an algorithm for deriving safe timing bounds of PPL programs will be defined. The analysis will be based on the abstraction of the PPL semantics presented in Chapter 5.

*NOTE. A summary of the notation and nomenclature used in this thesis can be found in Appendix A.*

### 6.1 Abstract Execution

ABSEXE, as given by Algorithm 6.1, can be used to derive safe approximations of the concrete final states resulting from a finite transition sequence (Lemma 6.8). ABSEXE will also safely approximate some infinite transition sequences but is not guaranteed to terminate for all possible inputs. The algorithm is a work-list algorithm and is defined based on the auxiliary functions CHOOSE, which returns an arbitrary element of a given set (which must be non-empty), ISFINAL, ISDEADLOCK, ISTIMEOUT, ISVALID, CYCLE, EXELoadThrd, GLOBALVAR, EXETHRD, GETVARLOAD and GETREGLOAD, defined in Algorithms 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8, 6.9, 6.10, 6.11 and 6.12,

**Algorithm 6.1** Abstract Execution

---

```

1: function ABSEXE( $\tilde{C}, \tilde{t}_{to}$ )
2:    $\tilde{C}^w \leftarrow \tilde{C}$ ;  $\tilde{C}^f \leftarrow \emptyset$ ;  $\tilde{C}^d \leftarrow \emptyset$ ;  $\tilde{C}^t \leftarrow \emptyset$ 
3:   while  $\tilde{C}^w \neq \emptyset$  do
4:      $\tilde{c} @ \langle [T, pc_T, \tilde{\pi}_T, \tilde{t}_T^a]_{T \in \text{Thrd}_e}, \tilde{x}, \tilde{\mathbb{I}} \rangle \leftarrow \text{CHOOSE}(\tilde{C}^w)$ 
5:      $\tilde{C}^w \leftarrow \tilde{C}^w \setminus \{\tilde{c}\}$ 
6:     if ISFINAL( $\tilde{c}$ ) then
7:        $\tilde{C}^f \leftarrow \tilde{C}^f \cup \{\tilde{c}\}$ 
8:     else if ISDEADLOCK( $\tilde{c}$ ) then
9:        $\tilde{C}^d \leftarrow \tilde{C}^d \cup \{\tilde{c}\}$ 
10:    else if ISTIMEOUT( $\tilde{c}, \tilde{t}_{to}$ ) then
11:       $\tilde{C}^t \leftarrow \tilde{C}^t \cup \{\tilde{c}\}$ 
12:    else if ISVALID( $\tilde{c}, \tilde{t}_{to}$ ) then
13:       $\text{Thrd}_{exe}^{\text{load}} \leftarrow \text{EXELoadThrd}(\tilde{c})$ 
14:      if  $|\text{Thrd}_{exe}^{\text{load}}| \neq \emptyset \wedge |\text{EXETHRD}(\tilde{c})| > 1$  then
15:         $\langle [\tilde{t}_T^a]_{T \in \text{Thrd}_{exe}^{\text{load}}} \rangle \leftarrow \langle [\tilde{t}_T^a \uparrow_t \text{ABSTIME}(\tilde{c}, T)]_{T \in \text{Thrd}_{exe}^{\text{load}}} \rangle$ 
16:        for all  $T \in \text{Thrd}_{exe}^{\text{load}}$  do
17:           $x \leftarrow \text{GETVARLOAD}(\text{STM}(T, pc_T))$ 
18:           $r \leftarrow \text{GETREGLOAD}(\text{STM}(T, pc_T))$ 
19:           $\tilde{c}' \leftarrow \langle [T', pc_{T'}, \tilde{\pi}_{T'}, \tilde{t}_{T'}^a]_{T' \in \text{Thrd}_e \setminus \{T\}}, \tilde{x}, \tilde{\mathbb{I}} \rangle$ 
20:           $(\tilde{C}_T^f, \tilde{C}_T^d, \tilde{C}_T^t) \leftarrow \text{ABSEXE}(\{\tilde{c}'\}, \tilde{t}_T^a \uparrow_t (\tilde{t}_{to} \sqcup_t \alpha_t(\{-\infty\})))$ 
21:           $\tilde{\pi}_T \leftarrow \tilde{\pi}_T[r \mapsto \perp_{val}]$ 
22:          for all  $(\tilde{T}, \tilde{x}', \tilde{\mathbb{I}}') \in \tilde{C}_T^f \cup \tilde{C}_T^d \cup \tilde{C}_T^t \cup \{\tilde{c}\}$  do
23:             $\tilde{\pi}_T \leftarrow \tilde{\pi}_T[r \mapsto (\tilde{\pi}_T r) \sqcup_{val} \text{READ}(\tilde{x}', x, T, \tilde{t}_{T'}^a)]$ 
24:          end for
25:        end for
26:         $\langle [pc_T]_{T \in \text{Thrd}_{exe}^{\text{load}}} \rangle \leftarrow \langle [pc_T + 1]_{T \in \text{Thrd}_{exe}^{\text{load}}} \rangle$ 
27:         $\langle [\tilde{t}_T^a]_{T \in \text{Thrd}_{exe}^{\text{load}}} \rangle \leftarrow \langle [\tilde{t}_T^a]_{T \in \text{Thrd}_{exe}^{\text{load}}} \rangle$ 
28:         $\tilde{C}^w \leftarrow \tilde{C}^w \cup \{ \langle [T, pc_T, \tilde{\pi}_T, \tilde{t}_T^a]_{T \in \text{Thrd}_e}, \tilde{x}, \tilde{\mathbb{I}} \rangle \}$ 
29:      else
30:         $\tilde{C}^w \leftarrow \tilde{C}^w \cup \{ \tilde{c}' \in \text{Conf} \mid \tilde{c} \xrightarrow{pg} \tilde{c}' \}$ 
31:      end if
32:    end if
33:  end while
34:  return  $(\tilde{C}^f, \tilde{C}^d, \tilde{C}^t)$ 
35: end function

```

---

respectively.

A thread executing a load-statement on some global variable (i.e., a variable that could transfer data between threads) is extracted and handled separately in case it would not be the sole thread executed on a transition. This is done by recursively using ABSEXE for each such thread to simulate how the rest of the threads in the configuration can affect the read value. When the effects have been derived, they are merged and put in the target register for the thread that issues the load-statement. Next, a new configuration, in which the load-statements have been performed, is added to the work-list.

If no load-statement on some global variable is issued in any thread, or a thread issuing such a load-statement is the sole thread that will execute on a transition,  $\xrightarrow{pg}$  is used to derive a set of succeeding configurations, which are then added to the work-list.

---

**Algorithm 6.2** Choose an Element
 

---

1: **function** CHOOSE( $S$ )

**Require:**  $S \neq \emptyset$

2: **return** one of the elements in  $S$

3: **end function**

---

Given an abstract configuration,  $\tilde{c} \in \mathbf{C\ddot{o}nf}$ , ISFINAL( $\tilde{c}$ ) means that  $\tilde{c}$  is in the final state; i.e., all threads issue halt-statements.

---

**Algorithm 6.3** Final Abstract Configuration
 

---

1: **function** ISFINAL( $\langle [T, pc_T, \tilde{x}_T, \tilde{I}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{I} \rangle$ )

2: **return**  $\forall T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc_T) = [\text{halt}]^{pc_T}$

3: **end function**

---

Given an abstract configuration,  $\tilde{c} \in \mathbf{C\ddot{o}nf}$ , ISDEADLOCK( $\tilde{c}$ ) means that  $\tilde{c}$  cannot reach a final state (Lemma 6.5). Note that ISDEADLOCK is not guaranteed to identify all such cases, though.

Given an abstract configuration,  $\tilde{c} \in \mathbf{C\ddot{o}nf}$ , and a timeout,  $\tilde{t}_{io} \in \mathbf{Ti\ddot{m}e}$ , ISTIMEOUT( $\tilde{c}, \tilde{t}_{io}$ ) means that  $\tilde{c}$  cannot reach a final state before  $\tilde{t}_{io}$  has passed (Lemma 6.6). Note that ISTIMEOUT might not identify all possible such cases, though.

Given an abstract configuration,  $\tilde{c} \in \mathbf{C\ddot{o}nf}$ , and a timeout,  $\tilde{t}_{io} \in \mathbf{Ti\ddot{m}e}$ ,  $\neg \text{ISVALID}(\tilde{c}, \tilde{t}_{io})$  means that  $\tilde{c}$  cannot reach a configuration that could represent at least one valid (c.f., Definition 4.4) concrete configuration (Lemma 6.7). Note that ISVALID might not identify all possible such cases, though.

---

**Algorithm 6.4** Deadlocked Abstract Configuration

---

1: **function** ISDEADLOCK( $\tilde{c}@\langle [T, pc_T, \tilde{\pi}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle$ )  
**Require:**  $\neg \text{ISFINAL}(\tilde{c})$   
2:  $\mathbf{Thrd}_{\text{lock}} \leftarrow \{T \in \mathbf{Thrd}_{\tilde{c}} \mid \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{OWN}(\tilde{l} \text{ lck}) \notin \{\perp_{\text{thrd}}, T\} \wedge \text{STT}(\tilde{l} \text{ lck}) = \text{locked})\}$   
3:  $E \leftarrow \{(T, T') \in \mathbf{Thrd}_{\text{lock}} \times \mathbf{Thrd}_{\text{lock}} \mid \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{OWN}(\tilde{l} \text{ lck}) = T')\}$   
4: **return**  $\mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd} \wedge (\text{CYCLE}(\mathbf{Thrd}_{\text{lock}}, E) \vee \exists T \in \mathbf{Thrd}_{\tilde{c}} : \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{STT}(\tilde{l} \text{ lck}) = \text{locked} \wedge \text{OWN}(\tilde{l} \text{ lck}) \neq \perp_{\text{thrd}} \wedge \text{STM}(\text{OWN}(\tilde{l} \text{ lck}), pc_{\text{OWN}(\tilde{l} \text{ lck})}) = [\text{halt}]^{pc_{\text{OWN}(\tilde{l} \text{ lck})}}))$   
5: **end function**

---



---

**Algorithm 6.5** Timed-Out Abstract Configuration

---

1: **function** ISTIMEOUT( $\tilde{c}@\langle [T, pc_T, \tilde{\pi}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle, \tilde{t}_{to}$ )  
**Require:**  $\neg \text{ISFINAL}(\tilde{c}) \wedge \neg \text{ISDEADLOCK}(\tilde{c})$   
2: **return**  $\forall T \in \mathbf{Thrd}_{\tilde{c}} : (\text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T} \Rightarrow (\tilde{t}_{to} \prec_t (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T)) \vee (\mathbf{Thrd}_{\tilde{c}} \subset \mathbf{Thrd} \wedge \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{OWN}(\tilde{l} \text{ lck}) \notin \{\perp_{\text{thrd}}, T\})))$   
3: **end function**

---



---

**Algorithm 6.6** Valid Abstract Configuration

---

1: **function** ISVALID( $\tilde{c}@\langle [T, pc_T, \tilde{\pi}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle, \tilde{t}_{to}$ )  
**Require:**  $\neg \text{ISFINAL}(\tilde{c}) \wedge \neg \text{ISDEADLOCK}(\tilde{c}) \wedge \neg \text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{to})$   
2:  $\mathbf{Thrd}_{\text{lock}} \leftarrow \{T \in \mathbf{Thrd}_{\tilde{c}} \mid \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{OWN}(\tilde{l} \text{ lck}) \notin \{\perp_{\text{thrd}}, T\})\}$   
3:  $E \leftarrow \{(T, T') \in \mathbf{Thrd}_{\text{lock}} \times \mathbf{Thrd}_{\text{lock}} \mid \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{OWN}(\tilde{l} \text{ lck}) = T')\}$   
4: **return**  $(\mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd} \Rightarrow \neg \text{CYCLE}(\mathbf{Thrd}_{\text{lock}}, E)) \wedge \forall lck \in \mathbf{Lck} : \forall T \in \mathbf{Thrd}_{\tilde{c}} : ((\text{OWN}(\tilde{l} \text{ lck}) = T \wedge \text{STT}(\tilde{l} \text{ lck}) = \text{unlocked}) \Rightarrow (\text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T} \wedge \text{DL}(\tilde{l} \text{ lck}) \prec_t (\tilde{t}_T^a \dot{+}_t \text{ABSTIME}(\tilde{c}, T))))$   
5: **end function**

---

Given a graph,  $(V, E)$ ,  $\text{CYCLE}(V, E)$  means that  $(V, E)$  contains at least one cycle (Lemma 6.1).

---

**Algorithm 6.7** Determine if Graph Has Cycles

---

```

1: function CYCLE( $V, E$ )
2:    $V' \leftarrow V$ 
3:    $E' \leftarrow E$ 
4:   while  $V' \neq \emptyset$  do
5:      $V'' \leftarrow \{v \in V' \mid \neg \exists v' \in V' : (v', v) \in E'\}$ 
6:     if  $V'' = \emptyset$  then
7:       return true
8:     else
9:        $E' \leftarrow E' \setminus \{(v, v') \in E' \mid v \in V'' \wedge v' \in V'\}$ 
10:       $V' \leftarrow V' \setminus V''$ 
11:    end if
12:  end while
13:  return false
14: end function
    
```

---

Given a configuration,  $\tilde{c} \in \mathbf{C\ddot{o}nf}$ ,  $\text{EXELoadThrd}(\tilde{c})$  is a set of threads that might issue a load-statement on a global variable in a transition from  $\tilde{c}$  (Lemma 6.4).

---

**Algorithm 6.8** Threads Executing a Possibly Unsafe Load Statement

---

```

1: function EXELoadThrd( $\tilde{c} @ \langle [T, pc_T, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle$ )
2:   return  $\{T \in \text{EXETHRD}(\tilde{c}) \mid \exists r \in \mathbf{Reg}_T : \exists x \in \text{GLOBALVAR}(\mathbf{Thrd}_{\tilde{c}}) : \text{STM}(T, pc_T) = [\text{load } r \text{ from } x]^{pc_T}\}$ 
3: end function
    
```

---

Given a set of threads,  $\mathbf{Thrd}_{\tilde{c}} \subseteq \mathbf{Thrd}$ ,  $\text{GLOBALVAR}(\mathbf{Thrd}_{\tilde{c}})$  is the set of variables that could transfer data between some of the threads in  $\mathbf{Thrd}_{\tilde{c}}$  (Lemma 6.3).

Given a configuration,  $\tilde{c} \in \mathbf{C\ddot{o}nf}$ ,  $\text{EXETHRD}(\tilde{c})$  is an over-approximation of  $\mathbf{Thrd}_{\text{exe}}$  as defined in Table 5.6 (Lemma 6.2).

Given a load-statement,  $\text{GETVARLOAD}$  is the variable, and  $\text{GETREGLOAD}$  is the register, defined by the statement.

**Lemma 6.1 (Soundness of CYCLE):**

Given the graph  $(V, E)$ , where  $V$  is a set of vertices and  $E$  is a set of edges (i.e.,

**Algorithm 6.9** Global Variables in an Abstract Configuration

---

```

1: function GLOBALVAR( $\text{Thrd}_{\tilde{c}}$ )
2:    $\langle [\text{Var}_{\text{T}}^{\text{load}}]_{\text{T} \in \text{Thrd}_{\tilde{c}}} \rangle \leftarrow$ 
      $\langle \{ \{ x \in \text{Var} \mid \exists r \in \text{Reg}_{\text{T}} : \exists l \in \text{Lbl}_{\text{T}} : \text{STM}(\text{T}, l) = [\text{load } r \text{ from } x]^l \} \}_{\text{T} \in \text{Thrd}_{\tilde{c}}} \rangle$ 
3:    $\langle [\text{Var}_{\text{T}}^{\text{store}}]_{\text{T} \in \text{Thrd}_{\tilde{c}}} \rangle \leftarrow$ 
      $\langle \{ \{ x \in \text{Var} \mid \exists r \in \text{Reg}_{\text{T}} : \exists l \in \text{Lbl}_{\text{T}} : \text{STM}(\text{T}, l) = [\text{store } r \text{ to } x]^l \} \}_{\text{T} \in \text{Thrd}_{\tilde{c}}} \rangle$ 
4:   return  $\{ x \in \text{Var} \mid \exists \text{T}, \text{T}' \in \text{Thrd}_{\tilde{c}} : (\text{T} \neq \text{T}' \wedge x \in \text{Var}_{\text{T}}^{\text{load}} \wedge x \in \text{Var}_{\text{T}'}^{\text{store}}) \}$ 
5: end function

```

---

**Algorithm 6.10** Threads to Execute in Abstract Configuration

---

```

1: function EXETHRD( $\tilde{c} @ \langle [\text{T}, pc_{\text{T}}, \tilde{\text{t}}_{\text{T}}, \tilde{t}_{\text{T}}^a]_{\text{T} \in \text{Thrd}_{\tilde{c}}}, \tilde{\text{x}}, \tilde{\text{l}} \rangle$ )
2:    $\text{Thrd}_{\text{hold}} \leftarrow \{ \text{T} \in \text{Thrd}_{\tilde{c}} \mid \text{STM}(\text{T}, pc_{\text{T}}) = [\text{halt}]^{pc_{\text{T}}} \vee \exists lck \in \text{Lck} :$ 
      $(\text{STM}(\text{T}, pc_{\text{T}}) = [\text{lock } lck]^{pc_{\text{T}}} \wedge \text{OWN}(\tilde{\text{l}} \text{ lck}) \neq \text{T}) \}$ 
3:    $\langle [\tilde{t}_{\text{T}}^r]_{\text{T} \in \text{Thrd}_{\tilde{c}} \setminus \text{Thrd}_{\text{hold}}} \rangle \leftarrow \langle [\text{ABSTIME}(\tilde{c}, \text{T})]_{\text{T} \in \text{Thrd}_{\tilde{c}} \setminus \text{Thrd}_{\text{hold}}} \rangle$ 
4:    $t_{\text{min}} \leftarrow \min \{ \min \{ \gamma_t(\tilde{t}_{\text{T}}^a \tilde{r}_t \tilde{t}_{\text{T}}^r) \mid \text{T} \in \text{Thrd}_{\tilde{c}} \setminus \text{Thrd}_{\text{hold}} \}$ 
5:    $t_{\text{max}} \leftarrow \min \{ \max \{ \gamma_t(\tilde{t}_{\text{T}}^a \tilde{r}_t \tilde{t}_{\text{T}}^r) \mid \text{T} \in \text{Thrd}_{\tilde{c}} \setminus \text{Thrd}_{\text{hold}} \}$ 
6:    $\tilde{t} \leftarrow \alpha_t(\{t_{\text{min}}, t_{\text{max}}\})$ 
7:   return  $\{ \text{T} \in \text{Thrd}_{\tilde{c}} \setminus \text{Thrd}_{\text{hold}} \mid \tilde{t} \uparrow_t (\tilde{t}_{\text{T}}^a \tilde{r}_t \tilde{t}_{\text{T}}^r) \neq \perp_t \} \cup$ 
      $\{ \text{T} \in \text{Thrd}_{\text{hold}} \mid \exists lck \in \text{Lck} :$ 
      $(\text{STM}(\text{T}, pc_{\text{T}}) = [\text{lock } lck]^{pc_{\text{T}}} \wedge \text{OWN}(\tilde{\text{l}} \text{ lck}) = \perp_{\text{thrd}}) \}$ 
8: end function

```

---

**Algorithm 6.11** Get Variable in Load Statement

---

```

1: function GETVARLOAD( $[\text{load } r \text{ from } x]^l$ )
2:   return  $x$ 
3: end function

```

---

**Algorithm 6.12** Get Register in Load Statement

---

```

1: function GETREGLOAD( $[\text{load } r \text{ from } x]^l$ )
2:   return  $r$ 
3: end function

```

---



pairs of vertices) connecting the vertices, then  $\text{CYCLE}(V, E)$  iff  $(V, E)$  contains at least one cycle.  $\square$

PROOF. Assume that  $(V, E)$  is a graph, where  $V$  is a set of vertices and  $E$  is a set of edges connecting the vertices. By definition, a cycle involving vertices  $v_1, v_2, v_3, \dots, v_n$  is described by the edges  $(v_1, v_2), (v_2, v_3), \dots, (v_n, v_1)$ , where  $n \geq 2$ . Thus it is easy to see that a vertex,  $v \in V$ , cannot be part of a cycle in  $(V, E)$  if  $\neg \exists v' \in V : (v', v) \in E$ ; i.e., if  $v$  has no incoming edges. It is also easy to see that the graph  $(V', E')$ , where  $V' = V \setminus \{v \in V \mid \neg \exists v' \in V : (v', v) \in E\}$  (i.e., all vertices without incoming edges are removed) and  $E' = E \setminus \{(v, v') \in E \mid v \in \{v'' \in V \mid \neg \exists v''' \in V : (v''', v'') \in E\} \wedge v' \in V\}$ , (i.e., all edges going out from a vertex without incoming edges are removed) contains exactly as many cycles as  $(V, E)$ .

Thus it must be that if this procedure can be repeated until an empty graph is reached, there are no cycles in the initial graph. Likewise, if it is not possible to reduce the initial graph to an empty graph, there must be at least one cycle in the initial graph. If there is no cycle in the initial graph, it is easy to see that the graph can be reduced to the empty graph by the above procedure. Likewise it is easy to see that if there is a cycle in the initial graph, the graph cannot be reduced to the empty graph by the above procedure. But then it must be that  $\text{CYCLE}(V, E)$  iff the graph  $(V, E)$  contains at least one cycle.  $\blacksquare$

**Lemma 6.2 (Soundness of EXETHRD):**

Given  $\tilde{c} \in \mathbf{C\ddot{o}nf}$ ,  $\mathbf{Thrd}_{exe}^{\tilde{c}} \subseteq \text{EXETHRD}(\tilde{c})$ , where  $\mathbf{Thrd}_{exe}^{\tilde{c}}$  is as defined in Table 5.6.  $\square$

PROOF. Based on  $\tilde{c} @ \langle [T, pc_T, \tilde{r}_T, \tilde{r}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle \in \mathbf{C\ddot{o}nf}$ , assume that  $\tilde{r}$  is as defined in Algorithm 6.10 and that  $\tilde{r}'$  is defined as  $\tilde{r}$  given by Table 5.6. It is easy to see that  $\mathbf{Thrd}_{hold}$  as given by Algorithm 6.10 is a superset of  $\mathbf{Thrd}_{hold}$  as given by Table 5.6 since in the latter case, a lock might have been assigned to some thread, which will exclude that thread from  $\mathbf{Thrd}_{hold}$ . Thus it must be that  $\min(\gamma_t(\tilde{r}')) \leq \min(\gamma_t(\tilde{r}))$  and  $\max(\gamma_t(\tilde{r}')) \leq \max(\gamma_t(\tilde{r}))$  (since  $\tilde{r}'$  is derived based on a superset of the threads used to derive  $\tilde{r}$ ; note that if it is a true superset, it must be that all the extra threads issue `lock lck` for some locks,  $lck \in \mathbf{Lck}$ , and have been assigned the ownership of  $lck$ , and that for those locks  $\text{OWN}(\tilde{l} lck) = \perp_{thrd}$ ). Thus it must be that  $\mathbf{Thrd}_{exe}^{\tilde{c}} \subseteq \text{EXETHRD}(\tilde{c})$ , where  $\mathbf{Thrd}_{exe}^{\tilde{c}}$  is as defined in Table 5.6, since  $\text{EXETHRD}(\tilde{c})$  is derived based on  $\tilde{r}$  but also includes all threads issuing `lock lck` where  $lck \in \mathbf{Lck}$  and  $\text{OWN}(\tilde{l} lck) = \perp_{thrd}$ .  $\blacksquare$

**Lemma 6.3 (Soundness of GLOBALVAR):**

$\text{GLOBALVAR}(\text{Thrd}_{\tilde{c}})$  is the set of variables (called global variables) for which a data dependency between two or more threads can occur in the program described by  $\text{Thrd}_{\tilde{c}}$ .  $\square$

PROOF. Assume that  $x \in \text{Var}$ . First note that

- if  $\{\text{T} \in \text{Thrd}_{\tilde{c}} \mid \exists l \in \text{Lbl}_{\text{T}} : \exists r \in \text{Reg}_{\text{T}} : [\text{store } r \text{ to } x]^l\} = \emptyset$  (i.e., no thread ever writes to  $x$ ), then it must be that  $x$  can be considered a constant (since  $x \in \text{Var}$ , there must be some thread reading from it),
- if  $\{\text{T} \in \text{Thrd}_{\tilde{c}} \mid \exists l \in \text{Lbl}_{\text{T}} : \exists r \in \text{Reg}_{\text{T}} : [\text{load } r \text{ from } x]^l\} = \emptyset$  (i.e., no thread ever reads from  $x$ ), then it must be that  $x$  can be considered a trash variable (since  $x \in \text{Var}$ , there must be some thread writing to it),
- if, for some thread,  $\text{T}' \in \text{Thrd}_{\tilde{c}}$ ,  $\{\text{T} \in \text{Thrd}_{\tilde{c}} \mid \exists l \in \text{Lbl}_{\text{T}} : \exists r \in \text{Reg}_{\text{T}} : [\text{store } r \text{ to } x]^l\} = \{\text{T}'\}$  and  $\{\text{T} \in \text{Thrd}_{\tilde{c}} \mid \exists l \in \text{Lbl}_{\text{T}} : \exists r \in \text{Reg}_{\text{T}} : [\text{load } r \text{ from } x]^l\} = \{\text{T}'\}$ , then it must be that  $x$  is only read from and written to by  $\text{T}'$  (thus there cannot be any data dependency on  $x$  between two threads), and
- for a data dependency to occur on  $x$  for two threads,  $\text{T}', \text{T}'' \in \text{Thrd}_{\tilde{c}}$ , it must be that  $\text{T}' \in \{\text{T} \in \text{Thrd}_{\tilde{c}} \mid \exists l \in \text{Lbl}_{\text{T}} : \exists r \in \text{Reg}_{\text{T}} : [\text{store } r \text{ to } x]^l\}$ ,  $\text{T}'' \in \{\text{T} \in \text{Thrd}_{\tilde{c}} \mid \exists l \in \text{Lbl}_{\text{T}} : \exists r \in \text{Reg}_{\text{T}} : [\text{load } r \text{ from } x]^l\}$  and  $\text{T}' \neq \text{T}''$ .

Thus, since for each  $\text{T} \in \text{Thrd}_{\tilde{c}}$ , the set  $\text{Var}_{\text{T}}^{\text{load}}$  contains all variables that  $\text{T}$  might read from and the set  $\text{Var}_{\text{T}}^{\text{store}}$  contains all variables that  $\text{T}$  might write to, it must be that  $\{x \in \text{Var} \mid \exists \text{T}', \text{T}'' \in \text{Thrd}_{\tilde{c}} : (\text{T}' \neq \text{T}'' \wedge x \in \text{Var}_{\text{T}'}^{\text{load}} \wedge x \in \text{Var}_{\text{T}''}^{\text{store}})\}$  is the set of variables for which data dependencies occur between at least two threads.  $\blacksquare$

**Lemma 6.4 (Soundness of EXELOADTHRD):**

Given a configuration  $\tilde{c} @ \langle [\text{T}, pc_{\text{T}}, \tilde{\text{r}}_{\text{T}}, \tilde{\text{i}}_{\text{T}}^a]_{\text{T} \in \text{Thrd}_{\tilde{c}}}, \tilde{\text{x}}, \tilde{\text{l}} \rangle \in \text{Cõnf}$ ,  $\{\text{T} \in \text{Thrd}_{\text{exe}}^{\tilde{c}} \mid \exists r \in \text{Reg}_{\text{T}} : \exists x \in \text{GLOBALVAR}(\text{Thrd}_{\tilde{c}}) : \text{STM}(\text{T}, pc_{\text{T}}) = [\text{load } r \text{ from } x]^{pc_{\text{T}}}\} \subseteq \text{EXELOADTHRD}(\tilde{c})$ , where  $\text{Thrd}_{\text{exe}}^{\tilde{c}}$  is defined as in Table 5.6.  $\square$

PROOF. Assume that  $\tilde{c} @ \langle [\text{T}, pc_{\text{T}}, \tilde{\text{r}}_{\text{T}}, \tilde{\text{i}}_{\text{T}}^a]_{\text{T} \in \text{Thrd}_{\tilde{c}}}, \tilde{\text{x}}, \tilde{\text{l}} \rangle \in \text{Cõnf}$  and that  $\text{Thrd}_{\text{exe}}^{\tilde{c}}$  is defined as in Table 5.6. The proof follows directly from the fact that  $\text{Thrd}_{\text{exe}}^{\tilde{c}} \subseteq \text{EXETHRD}(\tilde{c})$  (Lemma 6.2).  $\blacksquare$

**Lemma 6.5 (Soundness of ISDEADLOCK):**

Given a configuration  $\tilde{c} @ \langle [T, pc_T, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle \in \mathbf{C\ddot{on}f}$ , such that  $\exists T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}$ ,  $\text{ISDEADLOCK}(\tilde{c}) \Rightarrow \forall c \in \gamma_{\text{conf}}(\tilde{c}) : \neg \exists c' @ \langle [T, pc'_T, \tilde{x}'_T, \tilde{t}'_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}', \tilde{l}' \rangle \in \mathbf{C\ddot{on}f} : (c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \wedge \forall T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T})$ , where  $c$  and  $c'$  are valid concrete configurations (c.f., Definition 4.4); i.e., if  $\text{ISDEADLOCK}(\tilde{c})$ , then  $\tilde{c}$  does not represent any concrete configuration that can possibly reach a final state.  $\square$

PROOF. Assume that  $\tilde{c} @ \langle [T, pc_T, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle \in \mathbf{C\ddot{on}f}$ , such that  $\exists T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}$  (note that this assumption fulfills  $\neg \text{ISFINAL}(\tilde{c})$ ) and that  $\text{ISDEADLOCK}(\tilde{c})$ . Note that it must be that  $\mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd}$  (otherwise,  $\neg \text{ISDEADLOCK}(\tilde{c})$ ).

Since  $\mathbf{Thrd}_{\text{lock}} = \{T \in \mathbf{Thrd}_{\tilde{c}} \mid \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{O}\ddot{W}\text{N}(\tilde{l} \text{ lck}) \notin \{\perp_{\text{thrd}}, T\} \wedge \text{S}\ddot{T}\text{T}(\tilde{l} \text{ lck}) = \text{locked})\}$  and  $E = \{(T, T') \mid T, T' \in \mathbf{Thrd}_{\text{lock}} \wedge \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{O}\ddot{W}\text{N}(\tilde{l} \text{ lck}) = T')\}$ , it is easy to see that  $(\mathbf{Thrd}_{\text{lock}}, E)$  is a graph where the vertices (in  $\mathbf{Thrd}_{\text{lock}}$ ) represent threads that are waiting to acquire a lock that is currently acquired (i.e., owned and *locked*) by some other thread, and each edge,  $(T, T') \in E$ , describes a dependency (i.e.,  $T$  is waiting to acquire a lock that is currently acquired by  $T'$ ). But then it must be that if  $\text{CYCLE}(\mathbf{Thrd}_{\text{lock}}, E)$ , then for all  $c \in \gamma_{\text{conf}}(\tilde{c})$  (such that  $c$  is valid) there exists a deadlock in  $c$  (since  $(\mathbf{Thrd}_{\text{lock}}, E)$  contains at least one cycle; Lemma 6.1), and thus,  $\forall c \in \gamma_{\text{conf}}(\tilde{c}) : \neg \exists c' @ \langle [T, pc'_T, \tilde{x}'_T, \tilde{t}'_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}', \tilde{l}' \rangle \in \mathbf{C\ddot{on}f} : (c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \wedge \forall T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T})$ . (Note that if for some thread,  $T \in \mathbf{Thrd}_{\tilde{c}}$ , and lock,  $lck \in \mathbf{Lck}$ ,  $\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T}$ ,  $\text{O}\ddot{W}\text{N}(\tilde{l} \text{ lck}) \notin \{\perp_{\text{thrd}}, T\}$  and  $\text{S}\ddot{T}\text{T}(\tilde{l} \text{ lck}) = \text{unlocked}$ , then  $T \notin \mathbf{Thrd}_{\text{lock}}$  since  $\text{O}\ddot{W}\text{N}(\tilde{l} \text{ lck})$  has not yet acquired  $lck$ .)

If  $\exists T \in \mathbf{Thrd}_{\tilde{c}} : \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{S}\ddot{T}\text{T}(\tilde{l} \text{ lck}) = \text{locked} \wedge \text{O}\ddot{W}\text{N}(\tilde{l} \text{ lck}) \neq \perp_{\text{thrd}} \wedge \text{STM}(\text{O}\ddot{W}\text{N}(\tilde{l} \text{ lck}), pc_{\text{O}\ddot{W}\text{N}(\tilde{l} \text{ lck})}) = [\text{halt}]^{pc_{\text{O}\ddot{W}\text{N}(\tilde{l} \text{ lck})}})$ , it is easy to see that  $\text{O}\ddot{W}\text{N}(\tilde{l} \text{ lck})$  will never issue  $\text{unlock } lck$  (c.f., Tables 5.5 and 5.6) and thus  $\forall c \in \gamma_{\text{conf}}(\tilde{c}) : \neg \exists c' @ \langle [T, pc'_T, \tilde{x}'_T, \tilde{t}'_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}', \tilde{l}' \rangle \in \mathbf{C\ddot{on}f} : (c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \wedge \forall T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T})$ .

This concludes the proof.  $\blacksquare$

**Lemma 6.6 (Soundness of ISTIMEOUT):**

Given a configuration,  $\tilde{c} @ \langle [T, pc_T, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \tilde{x}, \tilde{l} \rangle \in \mathbf{C\ddot{on}f}$ , and time-out,  $\tilde{t}_{io} \in \mathbf{Time}$ , such that  $\exists T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}$  and  $\neg \text{ISDEADLOCK}(\tilde{c})$ ,  $\text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{io}) \Rightarrow \forall c \in \gamma_{\text{conf}}(\tilde{c}) : \neg \exists c' @$

$\langle [T, pc'_T, \mathbb{r}'_T, t^a_T]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : (c \xrightarrow{prg} \dots \xrightarrow{prg} c' \wedge \forall T \in \mathbf{Thrd}_{\tilde{c}} : (\text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T} \wedge t^a_T \leq \max(\gamma_t(\tilde{t}_{io}))))$ , where  $c$  and  $c'$  are valid concrete configurations (c.f., Definition 4.4); i.e., if  $\text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{io})$ , then  $\tilde{c}$  does not represent any concrete configuration that can possibly reach a final state before the given timeout (i.e., before  $\max(\gamma_t(\tilde{t}_{io}))$ ).  $\square$

PROOF. Assume that  $\tilde{c} @ \langle [T, pc_T, \mathbb{r}_T, t^a_T]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$  and  $\tilde{t}_{io} \in \mathbf{Time}$  are such that  $\exists T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}, \neg \text{ISDEADLOCK}(\tilde{c})$  and  $\text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{io})$ .

Since  $\text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{io})$ , it must be that  $\forall T \in \mathbf{Thrd}_{\tilde{c}} : (\text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T} \Rightarrow (\tilde{t}_{io} \prec_t (\tilde{t}^a_T \dot{\vdash}_t \text{ABSTIME}(\tilde{c}, T)) \vee (\mathbf{Thrd}_{\tilde{c}} \subset \mathbf{Thrd} \wedge \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{OWN}(\mathbb{l} \ lck) \notin \{\perp_{thrd}, T\}))))$ . For all threads,  $T \in \mathbf{Thrd}_{\tilde{c}}$ , such that  $\text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T} \wedge \tilde{t}_{io} \prec_t (\tilde{t}^a_T \dot{\vdash}_t \text{ABSTIME}(\tilde{c}, T))$ , it is easy to see that  $\neg \exists c' @ \langle [T, pc'_T, \mathbb{r}'_T, t^a_T]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : (c \xrightarrow{prg} \dots \xrightarrow{prg} c' \wedge \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T} \wedge t^a_T \leq \max(\gamma_t(\tilde{t}_{io})))$  (c.f., Assumptions 4.1 and 5.50). Thus, for all other threads,  $T \in \mathbf{Thrd}_{\tilde{c}}$ , such that  $\exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T) = [\text{lock } lck]^{pc_T} \wedge \text{OWN}(\mathbb{l} \ lck) \notin \{\perp_{thrd}, T\})$ , it must be that  $\neg \exists c' @ \langle [T, pc'_T, \mathbb{r}'_T, t^a_T]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : (c \xrightarrow{prg} \dots \xrightarrow{prg} c' \wedge \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T} \wedge t^a_T \leq \max(\gamma_t(\tilde{t}_{io})))$  since the respective locks cannot possibly be released at any time,  $t$ , such that  $t \leq \max(\gamma_t(\tilde{t}_{io}))$  (c.f., Assumptions 4.1 and 5.50).

This concludes the proof.  $\blacksquare$

**Lemma 6.7 (Soundness of ISVALID):**

Given a configuration  $\tilde{c} @ \langle [T, pc_T, \mathbb{r}_T, t^a_T]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$  and a time,  $\tilde{t}_{io} \in \mathbf{Time}$ , such that  $\exists T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}, \neg \text{ISDEADLOCK}(\tilde{c})$  and  $\neg \text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{io}), \neg \text{ISVALID}(\tilde{c}, \tilde{t}_{io}) \Rightarrow \neg \exists \tilde{c}' \in \mathbf{Conf} : (\tilde{c} \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}' \wedge \exists c @ \langle [T, pc_T, \mathbb{r}_T, t^a_T]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}, \mathbb{l} \rangle \in \gamma_{conf}(\tilde{c}') : (\exists c' \in \mathbf{Conf} : c' \xrightarrow{prg} \dots \xrightarrow{prg} c \wedge \forall lck \in \mathbf{Lck} : (\text{STT}(\mathbb{l} \ lck) = \text{unlocked} \Rightarrow \text{OWN}(\mathbb{l} \ lck) = \perp_{thrd})))$ ; i.e.,  $\tilde{c}$  can never lead to a configuration that could represent at least one valid concrete configuration (c.f., Definition 4.4).  $\square$

PROOF. Assume that  $\tilde{c} @ \langle [T, pc_T, \mathbb{r}_T, t^a_T]_{T \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{x}, \mathbb{l} \rangle \in \mathbf{Conf}$  and  $\tilde{t}_{io} \in \mathbf{Time}$  are such that  $\exists T \in \mathbf{Thrd}_{\tilde{c}} : \text{STM}(T, pc_T) \neq [\text{halt}]^{pc_T}, \neg \text{ISDEADLOCK}(\tilde{c}), \neg \text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{io})$  and  $\neg \text{ISVALID}(\tilde{c}, \tilde{t}_{io})$ . Then it must be that

1.  $\neg(\mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd} \Rightarrow \neg \text{CYCLE}(\mathbf{Thrd}_{\text{lock}}, E))$  (i.e.,  $\mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd} \wedge \text{CYCLE}(\mathbf{Thrd}_{\text{lock}}, E)$ ), where  $\mathbf{Thrd}_{\text{lock}} = \{T \in \mathbf{Thrd}_{\tilde{c}} \mid \exists lck \in$

$\mathbf{Lck} : (\text{STM}(\mathbf{T}, pc_{\mathbf{T}}) = [\text{lock } lck]^{pc_{\mathbf{T}}} \wedge \text{OWN}(\tilde{\mathbb{I}} lck) \notin \{\perp_{\text{thrd}}, \mathbf{T}\})$   
 and  $E = \{(\mathbf{T}, \mathbf{T}') \mid \mathbf{T}, \mathbf{T}' \in \mathbf{Thrd}_{\text{lock}} \wedge \exists lck \in \mathbf{Lck} : (\text{STM}(\mathbf{T}, pc_{\mathbf{T}}) = [\text{lock } lck]^{pc_{\mathbf{T}}} \wedge \text{OWN}(\tilde{\mathbb{I}} lck) = \mathbf{T}')\}$ , or

2.  $\neg \forall lck \in \mathbf{Lck} : \forall \mathbf{T} \in \mathbf{Thrd}_{\tilde{c}} : ((\text{OWN}(\tilde{\mathbb{I}} lck) = \mathbf{T} \wedge \text{STT}(\tilde{\mathbb{I}} lck) = \text{unlocked}) \Rightarrow (\text{STM}(\mathbf{T}, pc_{\mathbf{T}}) \neq [\text{halt}]^{pc_{\mathbf{T}}} \wedge \text{DL}(\tilde{\mathbb{I}} lck) \not\prec_t (\tilde{t}_{\mathbf{T}}^a \tilde{\dagger}_t \text{ABSTIME}(\tilde{c}, \mathbf{T}))))$ .

If  $\mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd} \wedge \text{CYCLE}(\mathbf{Thrd}_{\text{lock}}, E)$ , then it must be that there is a cycle in the dependency graph,  $(\mathbf{Thrd}_{\text{lock}}, E)$ , for threads waiting to acquire some lock (Lemma 6.1). Since  $\neg \text{ISDEADLOCK}(\tilde{c})$ , it must be that this cycle involves at least one lock,  $lck \in \mathbf{Lck}$ , such that for some thread,  $\mathbf{T} \in \mathbf{Thrd}$ ,  $\text{OWN}(\tilde{\mathbb{I}} lck) \notin \{\perp_{\text{thrd}}, \mathbf{T}\}$  and  $\text{STT}(\tilde{\mathbb{I}} lck) = \text{unlocked}$  (c.f., Algorithm 6.4). But then it is easy to see that  $\neg \exists \tilde{c}' \in \mathbf{Conf} : (\tilde{c} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}' \wedge \exists c @ \langle [\mathbf{T}, pc_{\mathbf{T}}, \mathbf{r}_{\mathbf{T}}, t_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{X}, \mathbb{I} \rangle \in \gamma_{\text{conf}}(\tilde{c}') : (\exists c' \in \mathbf{Conf} : c' \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c \wedge \forall lck \in \mathbf{Lck} : (\text{STT}(\mathbb{I} lck) = \text{unlocked} \Rightarrow \text{OWN}(\mathbb{I} lck) = \perp_{\text{thrd}})))$  (c.f., Tables 5.5 and 5.6 and Lemma 4.5).

Note that if  $\neg \forall lck \in \mathbf{Lck} : \forall \mathbf{T} \in \mathbf{Thrd}_{\tilde{c}} : ((\text{OWN}(\tilde{\mathbb{I}} lck) = \mathbf{T} \wedge \text{STT}(\tilde{\mathbb{I}} lck) = \text{unlocked}) \Rightarrow (\text{STM}(\mathbf{T}, pc_{\mathbf{T}}) \neq [\text{halt}]^{pc_{\mathbf{T}}} \wedge \text{DL}(\tilde{\mathbb{I}} lck) \not\prec_t (\tilde{t}_{\mathbf{T}}^a \tilde{\dagger}_t \text{ABSTIME}(\tilde{c}, \mathbf{T}))))$ , then it must be that  $\exists lck \in \mathbf{Lck} : \exists \mathbf{T} \in \mathbf{Thrd}_{\tilde{c}} : (\text{OWN}(\tilde{\mathbb{I}} lck) = \mathbf{T} \wedge \text{STT}(\tilde{\mathbb{I}} lck) = \text{unlocked} \wedge (\text{STM}(\mathbf{T}, pc_{\mathbf{T}}) = [\text{halt}]^{pc_{\mathbf{T}}} \vee \text{DL}(\tilde{\mathbb{I}} lck) \prec_t (\tilde{t}_{\mathbf{T}}^a \tilde{\dagger}_t \text{ABSTIME}(\tilde{c}, \mathbf{T}))))$ .

If  $\exists lck \in \mathbf{Lck} : \exists \mathbf{T} \in \mathbf{Thrd}_{\tilde{c}} : (\text{OWN}(\tilde{\mathbb{I}} lck) = \mathbf{T} \wedge \text{STT}(\tilde{\mathbb{I}} lck) = \text{unlocked} \wedge \text{STM}(\mathbf{T}, pc_{\mathbf{T}}) = [\text{halt}]^{pc_{\mathbf{T}}})$ , then it is easy to see that  $\neg \exists \tilde{c}' \in \mathbf{Conf} : (\tilde{c} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}' \wedge \exists c @ \langle [\mathbf{T}, pc_{\mathbf{T}}, \mathbf{r}_{\mathbf{T}}, t_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{X}, \mathbb{I} \rangle \in \gamma_{\text{conf}}(\tilde{c}') : (\exists c' \in \mathbf{Conf} : c' \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c \wedge \forall lck \in \mathbf{Lck} : (\text{STT}(\mathbb{I} lck) = \text{unlocked} \Rightarrow \text{OWN}(\mathbb{I} lck) = \perp_{\text{thrd}})))$  since, for the given lock, the owner will be  $\mathbf{T}$  but the state will remain *unlocked* for all configurations following  $\tilde{c}$  (c.f., Tables 5.5 and 5.6).

If  $\exists lck \in \mathbf{Lck} : \exists \mathbf{T} \in \mathbf{Thrd}_{\tilde{c}} : (\text{OWN}(\tilde{\mathbb{I}} lck) = \mathbf{T} \wedge \text{STT}(\tilde{\mathbb{I}} lck) = \text{unlocked} \wedge \text{DL}(\tilde{\mathbb{I}} lck) \prec_t (\tilde{t}_{\mathbf{T}}^a \tilde{\dagger}_t \text{ABSTIME}(\tilde{c}, \mathbf{T})))$ , then it is easy to see that  $\neg \exists \tilde{c}' \in \mathbf{Conf} : (\tilde{c} \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} \tilde{c}' \wedge \exists c @ \langle [\mathbf{T}, pc_{\mathbf{T}}, \mathbf{r}_{\mathbf{T}}, t_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_{\tilde{c}}}, \mathbb{X}, \mathbb{I} \rangle \in \gamma_{\text{conf}}(\tilde{c}') : (\exists c' \in \mathbf{Conf} : c' \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c \wedge \forall lck \in \mathbf{Lck} : (\text{STT}(\mathbb{I} lck) = \text{unlocked} \Rightarrow \text{OWN}(\mathbb{I} lck) = \perp_{\text{thrd}})))$

since  $\text{OWN}(\tilde{\mathbb{I}} lck)$  must be one of the threads that issue `lock lck` (and thus determines  $\text{DL}(\mathbb{I} lck)$ ) in the concrete case for  $\forall lck \in \mathbf{Lck} : (\text{STT}(\mathbb{I} lck) = \text{unlocked} \Rightarrow \text{OWN}(\mathbb{I} lck) = \perp_{\text{thrd}})$  to hold. But since  $\text{DL}(\tilde{\mathbb{I}} lck) \prec_t (\tilde{t}_{\mathbf{T}}^a \tilde{\dagger}_t \text{ABSTIME}(\tilde{c}, \mathbf{T}))$  and  $\text{DL}(\mathbb{I} lck) \in \gamma_t(\text{DL}(\tilde{\mathbb{I}} lck))$  for any given transitional sequence (c.f., Lemma 5.58), there cannot be any  $c \in \gamma_{\text{conf}}(\tilde{c})$  such that  $\text{OWN}(\tilde{\mathbb{I}} lck) = \mathbf{T}$  (c.f., Assumptions 4.1 and 5.50 and Tables 4.2, 4.3, 5.5 and 5.6).

This concludes the proof. ■

**Lemma 6.8 (Soundness of ABSEXE):**

Given the sets of valid configurations  $C \in \mathcal{P}(\mathbf{Conf})$  (c.f., Definition 4.4) and  $\tilde{C} \in \mathcal{P}(\mathbf{Conf})$ , such that  $\forall c @ \langle [T, pc_T, r_T, t_T^a]_{T \in \mathbf{Thrd}_1}, \mathbb{x}, \mathbb{l} \rangle \in C : (\forall \langle [T, pc_T^{\tilde{c}}, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_2}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \tilde{C} : (\mathbf{Thrd}_1 = \mathbf{Thrd}_2 = \mathbf{Thrd}) \wedge \exists \tilde{c} \in \tilde{C} : c \in \gamma_{conf}(\tilde{c}) \wedge |\mathbf{Thrd}| < \infty \wedge \forall \tilde{c} @ \langle [T, pc_T^{\tilde{c}}, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \tilde{C} : \forall lck \in \mathbf{Lck} : \min(\gamma_t(\tilde{\mathbb{L}}(lck)) = -\infty))$ , and the times  $t_{io} \in \mathbf{Time}$  and  $\tilde{t}_{io} \in \mathbf{Time}$ , such that  $t_{io} = \max(\gamma_t(\tilde{t}_{io}))$ ,  $(\tilde{C}^f, \tilde{C}^d, \tilde{C}^t) @ \text{ABSEXE}(\tilde{C}, \tilde{t}_{io})$  is such that

$$\begin{aligned}
 & \forall c \in C : \forall c' @ \langle [T, pc'_T, r'_T, t'^a_T]_{T \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : \\
 & ((c \xrightarrow{prg} \dots \xrightarrow{prg} c' \wedge \forall T \in \mathbf{Thrd} : \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T}) \Rightarrow \\
 & (\tilde{C}^t \neq \emptyset \vee \\
 & \exists \tilde{c} @ \langle [T, pc_T^{\tilde{c}}, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \tilde{C}^f : \forall T \in \mathbf{Thrd} : \\
 & \quad (pc'_T = pc'_T \wedge t'^a_T \in \gamma_t(\tilde{t}_T^a))) \wedge \\
 & \forall c \in C : \forall c' @ \langle [T, pc'_T, r'_T, t'^a_T]_{T \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : \\
 & ((c \xrightarrow{prg} \dots \xrightarrow{prg} c' \wedge (\text{CYCLE}(\mathbf{Thrd}_{lock}^c, E^c) \vee \\
 & \exists T \in \mathbf{Thrd} : \exists lck \in \mathbf{Lck} : \\
 & \quad (\text{STM}(T, pc'_T) = [\text{lock } lck]^{pc'_T} \wedge \\
 & \quad \text{OWN}(\mathbb{l}' lck) \notin \{\perp_{thrd}, T\} \wedge \\
 & \quad \text{STM}(\text{OWN}(\mathbb{l}' lck), pc'_{\text{OWN}(\mathbb{l}' lck)}) = \\
 & \quad \quad [\text{halt}]^{pc'_{\text{OWN}(\mathbb{l}' lck)}})) \Rightarrow \\
 & (\tilde{C}^t \neq \emptyset \vee \tilde{C}^d \neq \emptyset))
 \end{aligned}$$

where  $\mathbf{Thrd}_{lock}^c = \{T \in \mathbf{Thrd} \mid \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc'_T) = [\text{lock } lck]^{pc'_T} \wedge \text{OWN}(\mathbb{l}' lck) \notin \{\perp_{thrd}, T\})\}$  and  $E^c = \{(T, T') \mid T, T' \in \mathbf{Thrd}_{lock}^c \wedge \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc'_T) = [\text{lock } lck]^{pc'_T} \wedge \text{OWN}(\mathbb{l}' lck) = T')\}$ , whenever it terminates. In other words, if a concrete configuration in  $C$  could be executed into a final configuration, ABSEXE will either find a final abstract configuration that safely represents the timing behavior of the concrete final configuration or reach a timeout for the corresponding abstract transition sequence, and thus,  $\tilde{C}^t \neq \emptyset$ . If a concrete configuration in  $C$  could be executed into a state from which a final configuration cannot be reached, ABSEXE will either find the corresponding abstract situation (i.e.,  $\tilde{C}^d \neq \emptyset$ ) or reach a timeout for the corresponding abstract transition sequence, and thus,  $\tilde{C}^t \neq \emptyset$ .

It is also the case that if  $\tilde{C}^d \cup \tilde{C}^t = \emptyset$ , then all concrete configurations in  $C$  are guaranteed to, along all possible paths, reach a state in which all threads issue the `halt`-statement (i.e., reach the final state, or in other words, terminate).

Furthermore (if  $\tilde{C}^d \cup \tilde{C}^t = \emptyset$ ):

$$\begin{aligned} & \forall c \in C : \forall c' @ \langle [\mathbf{T}, pc'_T, \mathbb{r}'_T, t'^a_T]_{\mathbf{T} \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : \\ & ((c \xrightarrow{prg} \dots \xrightarrow{prg} c' \wedge \forall \mathbf{T} \in \mathbf{Thrd} : \text{STM}(\mathbf{T}, pc'_T) = [\text{halt}]^{pc'_T}) \Rightarrow \\ & \quad \exists \langle [\mathbf{T}, pc^{\tilde{c}}_T, \tilde{\mathbb{r}}_T, \tilde{t}^a_T]_{\mathbf{T} \in \mathbf{Thrd}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \tilde{C}^f : (pc^{\tilde{c}}_T = pc'_T \wedge t^a_T \in \gamma_t(\tilde{t}^a_T))) \quad \square \end{aligned}$$

PROOF. Assume that the sets of valid configurations  $C \in \mathcal{P}(\mathbf{Conf})$  and  $\tilde{C} \in \mathcal{P}(\mathbf{Conf})$  are such that  $\forall c @ \langle [\mathbf{T}, pc_T, \mathbb{r}_T, t^a_T]_{\mathbf{T} \in \mathbf{Thrd}_1}, \mathbb{x}, \mathbb{l} \rangle \in C : (\forall \langle [\mathbf{T}, pc^{\tilde{c}}_T, \tilde{\mathbb{r}}_T, \tilde{t}^a_T]_{\mathbf{T} \in \mathbf{Thrd}_2}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \tilde{C} : (\mathbf{Thrd}_1 = \mathbf{Thrd}_2 = \mathbf{Thrd}) \wedge \exists \tilde{c} \in \tilde{C} : c \in \gamma_{conf}(\tilde{c}) \wedge |\mathbf{Thrd}| < \infty \wedge \forall \tilde{c} @ \langle [\mathbf{T}, pc^{\tilde{c}}_T, \tilde{\mathbb{r}}_T, \tilde{t}^a_T]_{\mathbf{T} \in \mathbf{Thrd}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \tilde{C} : \forall lck \in \mathbf{Lck} : \min(\gamma_t(\text{DL}(\tilde{\mathbb{l}} lck) = -\infty))$ , the times  $t_{io} \in \mathbf{Time}$  and  $\tilde{t}_{io} \in \mathbf{Time}$ , are such that  $t_{io} = \max(\gamma_t(\tilde{t}_{io}))$ , and that  $(\tilde{C}^f, \tilde{C}^d, \tilde{C}^t) = \text{ABSEXE}(\tilde{C}, \tilde{t}_{io})$ .

This proof will partly be conducted using induction on the considered level of recursion, where level 0 is the base level (i.e., the level where for any considered  $\tilde{c}$ ,  $\mathbf{Thrd}_{\tilde{c}} = \mathbf{Thrd}$ ) and level  $n \geq 0$  is the bottom level (i.e., the level from which no more recursion occurs, which is also referred to as the maximum level of recursion), while assuming that all sequentially preceding load-statements in all threads for any considered configuration on any level of recursion have been safely approximated. Before beginning the induction part of the proof, first note that:

- The overall structure of the algorithm is of the work-list type; i.e., given an item (abstract configuration in this case) that is extracted from a work-list, new items are generated, based on some rules, and are either added to the work-list (and will thus eventually be extracted themselves) or saved as output items if some condition is fulfilled. When the work-list is empty, the algorithm terminates.
- Since  $(\tilde{C}^f, \tilde{C}^d, \tilde{C}^t) = \text{ABSEXE}(\tilde{C}, \tilde{t}_{io})$ , it must be that the algorithm terminates for the considered input (i.e.,  $\tilde{C}$  and  $\tilde{t}_{io}$ ).
- The structure of the algorithm is such that, for any  $\tilde{c} \in \mathbf{Conf}$  and  $\tilde{t}_{io} \in \mathbf{Time}$ ,  $\text{ISDEADLOCK}(\tilde{c})$  is only issued when  $\neg \text{ISFINAL}(\tilde{c})$ ,  $\text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{io})$  is only issued when  $\neg \text{ISDEADLOCK}(\tilde{c})$ , and  $\text{ISVALID}(\tilde{c}, \tilde{t}_{io})$  is only issued when  $\neg \text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{io})$ . This means that the requirements of Algorithms 6.4, 6.5 and 6.6 are fulfilled.
- The timing behaviors of the threads included on any recursion level are safely given by  $\text{ABSTIME}$  (Assumption 5.50).

- The maximum level (i.e., depth) of any recursion pattern is  $|\mathbf{Thrd}| - 1$  since  $|\text{EXETHRD}(\tilde{c})| > 1$  for recursion to occur and  $|\mathbf{Thrd}| \geq |\text{EXETHRD}(\tilde{c})|$  for any  $\tilde{c} \in \mathbf{Conf}$  (c.f., Algorithm 6.10). Since  $|\mathbf{Thrd}| < \infty$ , it must thus be that  $0 \leq n \leq |\mathbf{Thrd}| - 1 < \infty$ . But then, since the recursion depth is of a finite size, it must be that the recursion eventually stops for any considered case.
- When the considered level of recursion,  $i$ , is greater than 0, it is easy to see that  $\mathbf{Thrd}_i \subset \mathbf{Thrd}$ , where  $\mathbf{Thrd}_i$  is the set of threads included in any configuration on recursion level  $i$  for the considered recursion pattern. Note that  $\mathbf{Thrd}_0 = \mathbf{Thrd}$ .
- The timeout,  $\tilde{t}_{to}^i$ , for recursion level  $i > 0$  is such that  $\max(\gamma_t(\tilde{t}_{to}^i)) \leq \max(\gamma_t(\tilde{t}_{to}^{i-1}))$  since  $\tilde{t}_{to}^i = \tilde{t}_{T'}^{a'} \uparrow_t (\tilde{t}_{to}^{i-1} \sqcup_t \alpha_t(\{-\infty\}))$ , where  $T \in \mathbf{Thrd}_{\tilde{c}}$  is the thread that will be removed from the configurations on recursion level  $i$ . This means that the timeout cannot be shifted into the future when recursion occurs.

Figure 6.1 illustrates a case where  $n = 4$ ,  $\tilde{t}_{to}^0$  is the timeout at the base level (i.e., recursion level 0) and for all  $i \in \{1, 2, 3, 4\}$ ,  $\tilde{t}_{to}^i$  is the timeout at recursion level  $i$ ,  $T_{i-1}$  is the thread not included in configurations at recursion level  $i$  and  $\tilde{t}_{T_{i-1}}^{a'} = \tilde{t}_{T_{i-1}}^a \uparrow_t \text{ABSTIME}(\tilde{c}^{i-1}, T_{i-1})$ .

- Assume that a thread,  $T \in \mathbf{Thrd}$ , issues a load-statement at some recursion level  $i - 2$ , where  $i \geq 2$ , and has been removed from all configurations at recursion level  $i - 1$  and beyond, and that no events occurring after  $\tilde{t}_{to}^{i-1}$  can affect the loaded value. If some other thread,  $T' \in \mathbf{Thrd}$ , issues a possibly unsafe load-statement at recursion level  $i - 1$ , then a new recursion level,  $i$ , will be created to determine a safe write history before the load in  $T'$  is evaluated. Then it is easy to see that any event occurring after  $\tilde{t}_{T'}^{a'}$  cannot affect the value loaded by  $T'$ . But then it is easy to see that the value loaded by  $T$  at recursion level  $i - 2$  cannot be affected by any event occurring after  $\tilde{t}_{to}^i = \tilde{t}_{T'}^{a'} \uparrow_t (\tilde{t}_{to}^{i-1} \sqcup_t \alpha_t(\{-\infty\}))$  for the considered recursion instance at level  $i$ . Thus, for all recursion levels  $i \in \{1, \dots, n\}$ , the timeout for recursion level  $i$ , as determined by the algorithm, is safe since the accumulated time for a thread cannot decrease (c.f., Assumption 5.50).
- The structure of the algorithm (i.e., on a recursion level, one new recursion-instance is created for each thread that is executing a possibly unsafe load-statement) gives that all possible cases, for in which order load-statements in different threads can be issued, are considered.



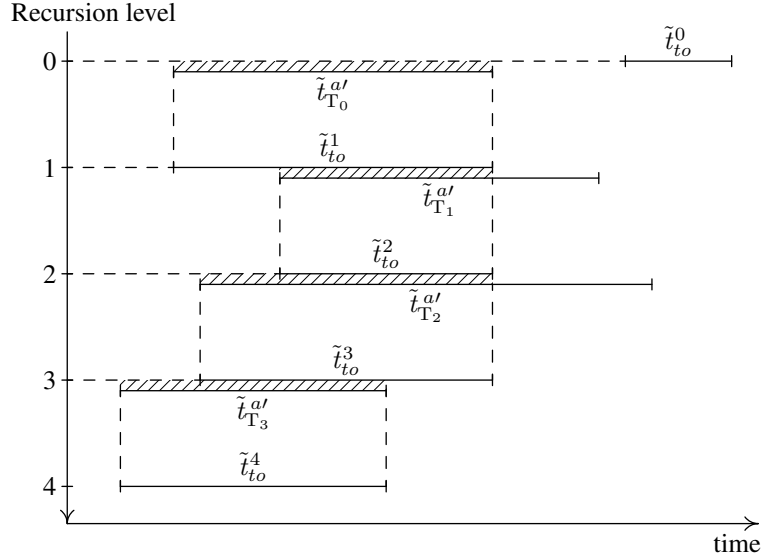


Figure 6.1: Illustration of how the timeout,  $\tilde{t}_{to}$ , for a new level of recursion in ABS\texttt{EXE} is determined.

Assume that, given some configuration,  $\tilde{c} @ \langle [\mathbf{T}, \rho c_{\mathbf{T}}^{\tilde{c}}, \tilde{\pi}_{\mathbf{T}}, \tilde{t}_{\mathbf{T}}^a]_{\mathbf{T} \in \mathbf{Thrd}_i}, \tilde{x}, \tilde{\mathbb{I}} \rangle$ , and timeout,  $\tilde{t}_{to}$ , on recursion level  $i$ , where  $0 \leq i < n$ , some thread,  $\mathbf{T}_i \in \mathbf{Thrd}_i$ , issues a possibly unsafe load-statement (which means that a deeper recursion level,  $i + 1$ , will exist) that cannot be affected by any event occurring after  $\tilde{t}_{to}$ . Further assume that the local thread states (i.e., program counters, register values and accumulated execution times) and write history for all variables as given by  $\tilde{c}$  safely approximate the possible concrete thread states and variable values given the considered program point and the corresponding concrete transition sequences (if any), and that all load-statements on recursion levels  $i + 1$  to  $n$  are safely approximated. This comprises the induction assumption.

Since the local thread states and write history for all variables as given by  $\tilde{c}$  safely approximate the possible concrete thread states and variable values given by the configuration at the end of the corresponding concrete transition sequences and all load-statements on recursion levels  $i + 1$  to  $n$  are safely approximated, it must be that all  $\tilde{c}' \in \mathbf{Conf}$ , such that  $\tilde{c} \xrightarrow{prg} \dots \xrightarrow{prg} \tilde{c}'$ , safely approximate the possible concrete thread states

and variable values given the considered program point and the corresponding concrete transition sequences since  $\xrightarrow{prg}$  is used to approximate the execution of all statements except load-statements that are possibly unsafe (c.f., Lemmas 5.55, 5.56 and 5.57). Thus, it must be that  $(\tilde{C}_{i+1}^f, \tilde{C}_{i+1}^d, \tilde{C}_{i+1}^t) @ \text{ABSEXE}(\{\langle [T, pc_T^c, \tilde{x}_T, \tilde{l}_T^a]_{T \in \text{Thrd}_i \setminus \{T_i\}}, \tilde{x}, \tilde{l} \rangle\}, (\tilde{t}_i^a \tilde{\tau}_t \text{ABSTIME}(\tilde{c}, T_i)) \uparrow_t (\tilde{t}_{io} \sqcup_t \alpha_t(\{-\infty\})))$  is such that  $\sqcup_{val} \{\text{READ}(\tilde{x}', x, T_i, \tilde{t}_T^a \tilde{\tau}_t \text{ABSTIME}(\tilde{c}, T_i)) \mid \langle \tilde{T}, \tilde{x}', \tilde{l}' \rangle \in \tilde{C}_{i+1}^f \cup \tilde{C}_{i+1}^d \cup \tilde{C}_{i+1}^t \cup \{\tilde{c}\}\}$  safely approximates all possible concrete values that could be read by the load-statement in  $T_i$  for the corresponding concrete transition sequence, since (the ABSEXE instance mentioned above, corresponding to recursion level  $i+1$  is considered)

1.  $\{\tilde{c}'' \in \mathbf{C\tilde{o}nf} \mid \tilde{c}' \xrightarrow{prg} \tilde{c}''\}$  safely collects all transition possibilities for any given configuration,  $\tilde{c}' \in \mathbf{C\tilde{o}nf}$ , or rather, thread, for which no possibly unsafe load-statements are approximated by the transition (c.f., Lemmas 5.55, 5.56 and 5.57),
2. TRIM is not used to remove old writes from the write history since  $i+1 > 0$  (c.f., Table 5.6),
3. (note that  $\mathbf{Thrd}_{i+1} \subset \mathbf{Thrd}$ )  $\forall \tilde{c}' @ \langle [T, pc_T^c, \tilde{x}'_T, \tilde{l}'_T^a]_{T \in \mathbf{Thrd}'}, \tilde{x}', \tilde{l}' \rangle \in \mathbf{C\tilde{o}nf} : (\mathbf{Thrd}' \subset \mathbf{Thrd} \Rightarrow \neg \text{ISDEADLOCK}(\tilde{c}'))$ ; i.e., even if a deadlock exists in  $\tilde{c}'$ , it is further evaluated just in case there are threads that are not part of the deadlock and thus could affect the value of the variable which is read on the lower recursion level (c.f., Algorithm 6.4),
4. for any  $\tilde{c}' \in \mathbf{C\tilde{o}nf}$  and  $\tilde{t}'_{io} \in \mathbf{Time}$ ,  $\text{ISTIMEOUT}(\tilde{c}', \tilde{t}'_{io}) \Rightarrow \forall c \in \gamma_{conf}(\tilde{c}') : \neg \exists c' @ \langle [T, pc_T^c, \tilde{x}'_T, \tilde{l}'_T^a]_{T \in \mathbf{Thrd}_{c'}}, \tilde{x}', \tilde{l}' \rangle \in \mathbf{C\tilde{o}nf} : (c \xrightarrow{prg} \dots \xrightarrow{prg} c' \wedge \forall T \in \mathbf{Thrd}_{c'} : (\text{STM}(T, pc_T^c) = [\text{halt}]^{pc_T^c} \wedge t_T^a \leq \max(\gamma_t(\tilde{t}'_{io}))))$ , where  $c$  and  $c'$  are valid concrete configurations (c.f., Definition 4.4); i.e., if  $\text{ISTIMEOUT}(\tilde{c}', \tilde{t}'_{io})$ , then  $\tilde{c}'$  does not represent any concrete configuration that can possibly reach a final state before the given timeout (Lemma 6.6), or in other words, no thread in  $\tilde{c}'$  can affect the system state so that the effects are visible at or before  $\tilde{t}'_{io}$  (c.f., Algorithm 6.5 and Assumption 5.50),
5. (note that  $\mathbf{Thrd}_{i+1} \subset \mathbf{Thrd}$ )  $\forall \tilde{c}' @ \langle [T, pc_T^c, \tilde{x}'_T, \tilde{l}'_T^a]_{T \in \mathbf{Thrd}'}, \tilde{x}', \tilde{l}' \rangle \in \mathbf{C\tilde{o}nf} : ((\mathbf{Thrd}' \subset \mathbf{Thrd} \wedge \neg \text{ISVALID}(\tilde{c}')) \Rightarrow \neg \forall lck \in \mathbf{Lck} : \forall T \in \mathbf{Thrd}' : ((\text{OWN}(\tilde{l}' lck) = T \wedge \text{STT}(\tilde{l}' lck) = \text{unlocked}) \Rightarrow (\text{STM}(T, pc_T^c) \neq [\text{halt}]^{pc_T^c} \wedge \text{DL}(\tilde{l}' lck) \not\leq_t (\tilde{t}_T^a \tilde{\tau}_t \text{ABSTIME}(\tilde{c}, T))))$ , which follows

directly from Algorithm 6.6 and means that there is no possibility that  $\tilde{c}'$  has any (or could lead to a configuration that has a) valid concrete counterpart (c.f., Definition 4.4 and the proof of Lemma 6.7).

It is important to notice that `IS_TIMEOUT` captures all configurations such that all threads have either executed beyond the timeout or are waiting to acquire a lock that is currently owned by a thread that has executed beyond the timeout or is also waiting to acquire some lock (c.f., Algorithm 6.5), which means that the first mentioned thread cannot possibly acquire the lock before the timeout has passed (c.f., Tables 5.5 and 5.6 and Assumption 5.50). This means that `IS_TIMEOUT` captures all deadlocked configurations, since `IS_DEADLOCK` does not capture any configuration at all when the considered recursion level is greater than 0 (c.f., Algorithm 6.4), and also all configurations allowed by `IS_INVALID`, although they lack valid concrete counterparts (c.f., Algorithm 6.6).

Since  $\tilde{t}'_{T_i} = \tilde{t}^a_{T_i} \dot{+}_t \text{ABSTIME}(\tilde{c}^i, T_i)$ ,  $pc'_{T_i} = pc_{T_i} + 1$  and  $\tilde{r}'_{T_i} = \tilde{r}_{T_i}[r \mapsto \bigsqcup_{\text{val}} \{\text{READ}(\tilde{x}', x, T_i, \tilde{t}^a_{T_i} \dot{+}_t \text{ABSTIME}(\tilde{c}^i, T_i)) \mid \langle \tilde{\mathbf{T}}, \tilde{x}', \tilde{\mathbf{I}}' \rangle \in \tilde{C}^f_{i+1} \cup \tilde{C}^d_{i+1} \cup \tilde{C}^t_{i+1} \cup \{\tilde{c}^i\}\}]$  (assuming that the possibly unsafe `load`-statement issued by  $T_i$  is  $[\text{load } r \text{ from } x]^{pc_{T_i}}$  for some  $r \in \mathbf{Reg}_{T_i}$  and  $x \in \mathbf{Var}$ ), it must thus be that the `load`-statement in thread  $T_i$  on recursion level  $i$  is safely approximated and that the new configuration, which is added to the work-list on line 28, therefore safely approximates the local thread states (i.e., program counters, register values and accumulated execution times) for all threads and the write history for all variables as given by the possible concrete thread states and variable values in the considered program point and the corresponding concrete transition sequences (if any). But this means that all possibly unsafe `load`-statements on recursion level  $i$  are safely approximated.

Now consider recursion level  $n$  (i.e., the level from which no more recursion will occur for a given recursion pattern, which is the base case for the induction part of the proof) for the first ever occurring recursion pattern for a given transition sequence, such that no potentially unsafe `load`-statement has yet been approximated. Since no potentially unsafe `load`-statement has yet been approximated and  $\forall c \in C : \exists \tilde{c} \in \tilde{C} : c \in \gamma_{\text{conf}}(\tilde{c})$ , it must be that any concrete state for all threads individually, and the write history for each variable, must be safely approximated up until the considered point of the considered transition sequence (since  $\xrightarrow{\text{prg}}$  has been safely used for all transitions and  $\{\tilde{c}' \in \mathbf{C\tilde{on}f} \mid \tilde{c} \xrightarrow{\text{prg}} \tilde{c}'\}$  collects all abstract transition possibilities for any given configuration,  $\tilde{c} \in \mathbf{C\tilde{on}f}$ , or rather, thread; c.f., Lemmas 5.55, 5.56 and 5.57). Since no more (i.e.,

deeper) recursion will occur, it must be that for any considered configuration,  $\tilde{c} @ \langle [T, pc_T, \tilde{\pi}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_n}, \tilde{\mathbb{X}}, \tilde{\mathbb{I}} \rangle \in \mathbf{C\tilde{on}f}$ , at level  $n$ ,  $|\mathbf{EXETHRD}(\tilde{c})| \neq 1$  or  $\mathbf{EXELOADTHRD}(\tilde{c}) = \emptyset$ . But since for any given configuration  $\tilde{c} @ \langle [T, pc_T, \tilde{\pi}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_\varepsilon}, \tilde{\mathbb{X}}, \tilde{\mathbb{I}} \rangle \in \mathbf{C\tilde{on}f}$ ,  $\mathbf{Thrd}_{exe}^{\tilde{c}} \subseteq \mathbf{EXETHRD}(\tilde{c})$  (Lemma 6.2) and  $\{T \in \mathbf{Thrd}_{exe}^{\tilde{c}} \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{GLOBALVAR}(\mathbf{Thrd}_{\tilde{c}}) : \mathbf{STM}(T, pc_T) = [\text{load } r \text{ from } x]^{pc_T}\} \subseteq \mathbf{EXELOADTHRD}(\tilde{c})$  (Lemma 6.4), where  $\mathbf{Thrd}_{exe}^{\tilde{c}}$  is as defined in Table 5.6, it must thus be that  $|\mathbf{Thrd}_{exe}^{\tilde{c}}| \neq 1 \vee \{T \in \mathbf{Thrd}_{exe}^{\tilde{c}} \mid \exists r \in \mathbf{Reg}_T : \exists x \in \mathbf{Var}_g : \mathbf{STM}(T, pc_T) = [\text{load } r \text{ from } x]^{pc_T}\} = \emptyset$  for all  $\tilde{c} \in \mathbf{C\tilde{on}f}$  at recursion level  $n$ . Thus, it must be that  $\{\tilde{c}' \in \mathbf{C\tilde{on}f} \mid \tilde{c} \xrightarrow{prg} \tilde{c}'\}$  will be safely used to collect all the possible transitions on recursion level  $n$  until all threads either reach the final state (i.e., issue `halt`-statements) or execute beyond the timeout (c.f., Lemmas 5.55, 5.56, 5.57, 5.58, 6.5, 6.6 and 6.7). But, then it must be that all the possible concrete transition sequences for each thread are safely approximated up until the timeout point (if ever reached, and if reached before the final state) since  $\forall c \in C : \exists \tilde{c} \in \tilde{C} : c \in \gamma_{conf}(\tilde{c})$ . This concludes the induction part of the proof.

Given  $c \in C$  and  $c' @ \langle [T, pc'_T, \pi'_T, t'^a]_{T \in \mathbf{Thrd}}, \mathbb{X}', \mathbb{I}' \rangle \in \mathbf{Conf}$ , the following concrete cases (corresponding to a terminating program, a program reaching a deadlocked state and a more general case of a non-terminating program, respectively) must be considered.

1. Assume that  $c \xrightarrow{prg} \dots \xrightarrow{prg} c' \wedge \forall T \in \mathbf{Thrd} : \mathbf{STM}(T, pc'_T) = [\text{halt}]^{pc'_T}$ .

Note that since all possible concrete transition sequences for each thread individually are safely approximated up until the timeout point and a final configuration is reached in the concrete case, there must be an abstract trace of transitions such that all configurations,  $\tilde{c} \in \mathbf{C\tilde{on}f}$ , on that trace are such that  $\neg \mathbf{ISDEADLOCK}(\tilde{c})$  (c.f., Algorithm 6.4 and Lemma 6.5) and  $\mathbf{ISVALID}(\tilde{c}, \tilde{t}_{to})$  (c.f., Algorithm 6.6 and Lemma 6.7). It must also be that, eventually, a configuration,  $\tilde{c} @ \langle [T, pc_{\tilde{T}}^{\tilde{c}}, \tilde{\pi}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{\mathbb{X}}, \tilde{\mathbb{I}} \rangle \in \mathbf{C\tilde{on}f}$ , for which either  $\forall T \in \mathbf{Thrd} : \mathbf{STM}(T, pc_{\tilde{T}}^{\tilde{c}}) = [\text{halt}]^{pc_{\tilde{T}}^{\tilde{c}}}$  or  $\forall T \in \mathbf{Thrd} : (\mathbf{STM}(T, pc_{\tilde{T}}^{\tilde{c}}) \neq [\text{halt}]^{pc_{\tilde{T}}^{\tilde{c}}} \Rightarrow \tilde{t}_{to} \prec_t \tilde{t}_T^a \nmid_t \mathbf{ABSTIME}(\tilde{c}, T))$  is derived along the corresponding (over-approximating) abstract trace of transitions.

If  $\forall T \in \mathbf{Thrd} : \mathbf{STM}(T, pc_{\tilde{T}}^{\tilde{c}}) = [\text{halt}]^{pc_{\tilde{T}}^{\tilde{c}}}$ , then it is easy to see that  $\mathbf{ISFINAL}(\tilde{c})$  (c.f., Algorithm 6.3), which means that  $\tilde{c} \in \tilde{C}^f$ . Thus, it must be that  $\exists \tilde{c}' @ \langle [T, pc_{\tilde{T}}^{\tilde{c}'}, \tilde{\pi}'_T, \tilde{t}'_T^a]_{T \in \mathbf{Thrd}}, \tilde{\mathbb{X}}', \tilde{\mathbb{I}}' \rangle \in \tilde{C}^f : \forall T \in \mathbf{Thrd} : (pc_{\tilde{T}}^{\tilde{c}'} = pc'_T \wedge t'^a \in \gamma_t(\tilde{t}'_T^a))$ .

If  $\exists T \in \mathbf{Thrd} : \text{STM}(T, pc_T^{\tilde{c}}) \neq [\text{halt}]^{pc_T^{\tilde{c}}} \wedge \forall T \in \mathbf{Thrd} : (\text{STM}(T, pc_T^{\tilde{c}}) \neq [\text{halt}]^{pc_T^{\tilde{c}}} \Rightarrow \tilde{t}_{to} \prec_t \tilde{t}_T^a \tilde{\tau}_T \text{ ABSTIME}(\tilde{c}, T))$ , then it is easy to see that  $\neg \text{ISFINAL}(\tilde{c})$ ,  $\neg \text{ISDEADLOCK}(\tilde{c})$  (since the program terminates in the concrete case) and  $\text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{to})$  (c.f., Algorithms 6.3 and 6.5), which means that  $\tilde{c} \in \tilde{C}'$ . Thus, it must be that  $\tilde{C}' \neq \emptyset$ .

2. Assume that  $c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \wedge (\text{CYCLE}(\mathbf{Thrd}_{\text{lock}}^{c'}, E^{c'}) \vee \exists T \in \mathbf{Thrd} : \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T^{c'}) = [\text{lock } lck]^{pc_T^{c'}} \wedge \text{OWN}(\mathbb{1}' lck) \notin \{\perp_{\text{thrd}}, T\} \wedge \text{STM}(\text{OWN}(\mathbb{1}' lck), pc_{\text{OWN}(\mathbb{1}' lck)}^{c'}) = [\text{halt}]^{pc_{\text{OWN}(\mathbb{1}' lck)}^{c'}}))$ , where  $\mathbf{Thrd}_{\text{lock}}^{c'} = \{T \in \mathbf{Thrd} \mid \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T^{c'}) = [\text{lock } lck]^{pc_T^{c'}} \wedge \text{OWN}(\mathbb{1}' lck) \notin \{\perp_{\text{thrd}}, T\})\}$  and  $E^{c'} = \{(T, T') \mid T, T' \in \mathbf{Thrd}_{\text{lock}}^{c'} \wedge \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T^{c'}) = [\text{lock } lck]^{pc_T^{c'}} \wedge \text{OWN}(\mathbb{1}' lck) = T')\}$  (remember that  $\text{OWN}(\mathbb{1}' lck) \neq \perp_{\text{thrd}} \Rightarrow \text{OWN}(\mathbb{1}' lck) = \text{locked}$  since  $c$  is valid and  $\xrightarrow{\text{prg}}$  preserves validity; c.f., Definition 4.4 and Lemma 4.5). Note that since all possible concrete transition sequences for each thread individually are safely approximated up until the timeout point and a deadlocked configuration is reached in the concrete case, there must be an abstract trace of transitions such that all configurations,  $\tilde{c} \in \mathbf{C\o n f}$ , on that trace are such that  $\neg \text{ISFINAL}(\tilde{c})$  (c.f., Algorithm 6.3) and  $\text{ISVALID}(\tilde{c}, \tilde{t}_{to})$  (c.f., Algorithm 6.6 and Lemma 6.7). It must also be that, eventually, a configuration,  $\tilde{c} @ \langle [T, pc_T^{\tilde{c}}, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{\mathbb{1}} \rangle \in \mathbf{C\o n f}$ , will be derived (along the corresponding, over-approximating abstract trace of transitions) for which either  $(\text{CYCLE}(\mathbf{Thrd}_{\text{lock}}^{\tilde{c}}, E^{\tilde{c}}) \vee \exists T \in \mathbf{Thrd} : \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T^{\tilde{c}}) = [\text{lock } lck]^{pc_T^{\tilde{c}}} \wedge \text{STT}(\tilde{\mathbb{1}} lck) = \text{locked} \wedge \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck) \neq \perp_{\text{thrd}} \wedge \text{STM}(\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck), pc_{\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck)}^{\tilde{c}}) = [\text{halt}]^{pc_{\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck)}^{\tilde{c}}}))$ , where  $\mathbf{Thrd}_{\text{lock}}^{\tilde{c}} = \{T \in \mathbf{Thrd} \mid \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T^{\tilde{c}}) = [\text{lock } lck]^{pc_T^{\tilde{c}}} \wedge \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck) \notin \{\perp_{\text{thrd}}, T\} \wedge \text{STT}(\tilde{\mathbb{1}} lck) = \text{locked})\}$  and  $E^{\tilde{c}} = \{(T, T') \mid T, T' \in \mathbf{Thrd}_{\text{lock}}^{\tilde{c}} \wedge \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T^{\tilde{c}}) = [\text{lock } lck]^{pc_T^{\tilde{c}}} \wedge \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck) = T')\}$ , or  $\forall T \in \mathbf{Thrd} : (\text{STM}(T, pc_T^{\tilde{c}}) \neq [\text{halt}]^{pc_T^{\tilde{c}}} \Rightarrow \tilde{t}_{to} \prec_t \tilde{t}_T^a \tilde{\tau}_T \text{ ABSTIME}(\tilde{c}, T)) \wedge \neg (\text{CYCLE}(\mathbf{Thrd}_{\text{lock}}^{\tilde{c}}, E^{\tilde{c}}) \vee \exists T \in \mathbf{Thrd} : \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T^{\tilde{c}}) = [\text{lock } lck]^{pc_T^{\tilde{c}}} \wedge \text{STT}(\tilde{\mathbb{1}} lck) = \text{locked} \wedge \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck) \neq \perp_{\text{thrd}} \wedge \text{STM}(\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck), pc_{\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck)}^{\tilde{c}}) = [\text{halt}]^{pc_{\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck)}^{\tilde{c}}}))$ .

If  $\text{CYCLE}(\mathbf{Thrd}_{\text{lock}}^{\tilde{c}}, E^{\tilde{c}}) \vee \exists T \in \mathbf{Thrd} : \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T^{\tilde{c}}) = [\text{lock } lck]^{pc_T^{\tilde{c}}} \wedge \text{STT}(\tilde{\mathbb{1}} lck) = \text{locked} \wedge \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{1}} lck) \neq \perp_{\text{thrd}} \wedge$

$\text{STM}(\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}}\ lck), pc_{\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}}\ lck)}^{\tilde{c}}) = [\text{halt}]^{pc_{\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}}\ lck)}^{\tilde{c}}}$ , then it is easy to see that  $\neg\text{ISFINAL}(\tilde{c})$  and  $\text{ISDEADLOCK}(\tilde{c})$  (c.f., Algorithm 6.4 and Lemma 6.5), which means that  $\tilde{C}^d \neq \emptyset$ .

If  $\forall T \in \mathbf{Thrd} : (\text{STM}(T, pc_T^{\tilde{c}}) \neq [\text{halt}]^{pc_T^{\tilde{c}}} \Rightarrow \tilde{t}_{io} \prec_t \tilde{t}_T^a \nmid_t \text{ABSTIME}(\tilde{c}, T) \wedge \neg(\text{CYCLE}(\mathbf{Thrd}_{\text{lock}}^{\tilde{c}}, E^{\tilde{c}}) \vee \exists T \in \mathbf{Thrd} : \exists lck \in \mathbf{Lck} : (\text{STM}(T, pc_T^{\tilde{c}}) = [\text{lock } lck]^{pc_T^{\tilde{c}}} \wedge \text{STT}(\tilde{\mathbb{I}}\ lck) = \text{locked} \wedge \text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}}\ lck) \neq \perp_{\text{thrd}} \wedge \text{STM}(\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}}\ lck), pc_{\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}}\ lck)}^{\tilde{c}}) = [\text{halt}]^{pc_{\text{O}\tilde{\text{W}}\text{N}(\tilde{\mathbb{I}}\ lck)}^{\tilde{c}}}))$ , then it is easy to see that  $\neg\text{ISFINAL}(\tilde{c})$ ,  $\neg\text{ISDEADLOCK}(\tilde{c})$  and  $\text{ISTIMEOUT}(\tilde{c}, \tilde{t}_{io})$  (c.f., Algorithm 6.5 and Lemma 6.6), which means that  $\tilde{C}^t \neq \emptyset$ .

To prove the last part of the lemma, assume that  $\tilde{C}^d \cup \tilde{C}^t = \emptyset$ . Since  $\forall \langle [T, pc_T^{\tilde{c}}, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{\mathbb{I}} \rangle \in \tilde{C}^f : \forall T \in \mathbf{Thrd} : \text{STM}(T, pc_T^{\tilde{c}}) = [\text{halt}]^{pc_T^{\tilde{c}}}$  (c.f., Algorithm 6.3) and  $\neg\text{ISVALID}(\tilde{c}, \tilde{t}_{io})$  only if  $\tilde{c}$  can never lead to a configuration that might have a valid concrete counterpart (Lemma 6.7), it is easy to see that all concrete executions of the configurations in  $C$  will terminate since all possible concrete transition sequences are safely approximated. Further assume that  $c \in C$  and  $c' @ \langle [T, pc'_T, x'_T, t'^a]_{T \in \mathbf{Thrd}}, x', l' \rangle \in \mathbf{Conf}$  are such that  $c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \wedge \forall T \in \mathbf{Thrd} : \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T}$ . Since  $\tilde{C}^d \cup \tilde{C}^t = \emptyset$  and  $\forall c \in C : \exists \tilde{c} \in \tilde{C} : c \in \gamma_{\text{conf}}(\tilde{c})$ , it is easy to see that  $\exists \langle [T, pc_T^{\tilde{c}}, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{\mathbb{I}} \rangle \in \tilde{C}^f : (pc_T^{\tilde{c}} = pc'_T \wedge t_T^a \in \gamma_t(\tilde{t}_T^a))$  since all possible concrete transition sequences are safely approximated.

This concludes the proof. ■

NOTE. *ABSEXE* has not been proven to terminate for all inputs. However, when it does terminate, it safely approximates the transition sequences for the corresponding concrete input set.

One case for which *ABSEXE* will not terminate is when some thread could execute an infinite amount of statements in zero amount of time; c.f., an infinite loop where all the statements of the loop could be executed without any progression of time.

**Algorithm 6.13** BCET/WCET Analysis

---

```

1: function ANALYSIS( $\tilde{C}, \tilde{t}_{to}$ )
2:    $(\tilde{C}^f, \tilde{C}^d, \tilde{C}^t) \leftarrow \text{ABSEXE}(\tilde{C}, \tilde{t}_{to})$ 
3:   if  $\tilde{C}^d \cup \tilde{C}^t \neq \emptyset$  then
4:     return  $(-\infty, \infty)$ 
5:   end if
6:    $BCET \leftarrow -\infty$ 
7:    $WCET \leftarrow -\infty$ 
8:   while  $\tilde{C}^f \neq \emptyset$  do
9:      $\tilde{c} @ \langle [T, pc_T, \tilde{t}_T, \tilde{t}_T^a]_{T \in \text{Thrd}}, \tilde{x}, \tilde{l} \rangle \leftarrow \text{CHOOSE}(\tilde{C}^f)$ 
10:     $\tilde{C}^f \leftarrow \tilde{C}^f \setminus \{\tilde{c}\}$ 
11:     $BCET_{\tilde{c}} \leftarrow \max(\{\min(\gamma_t(\tilde{t}_T^a)) \mid T \in \text{Thrd}\})$ 
12:     $WCET_{\tilde{c}} \leftarrow \max(\{\max(\gamma_t(\tilde{t}_T^a)) \mid T \in \text{Thrd}\})$ 
13:    if  $BCET > BCET_{\tilde{c}}$  then
14:       $BCET \leftarrow BCET_{\tilde{c}}$ 
15:    end if
16:    if  $WCET < WCET_{\tilde{c}}$  then
17:       $WCET \leftarrow WCET_{\tilde{c}}$ 
18:    end if
19:  end while
20:  return  $(BCET, WCET)$ 
21: end function

```

---

## 6.2 Timing Analysis

The BCET and WCET (c.f., Definition 6.9) of a program, given an initial system state, is safely derived by ANALYSIS, which is defined in Algorithm 6.13 (Lemma 6.10), whenever it terminates.

### Definition 6.9 (BCET and WCET):

The Best-Case Execution Time, *BCET*, and the Worst-Case Execution Time, *WCET*, of a given configuration,  $\langle [T, pc_T, \mathfrak{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_e}, \mathfrak{x}, \tilde{\mathbb{I}} \rangle \in \mathbf{C\ddot{on}f}$  are defined as:

$$\begin{cases} BCET = \max(\{\min(\gamma_t(\tilde{t}_T^a) \mid T \in \mathbf{Thrd}_e\}) \\ WCET = \max(\{\max(\gamma_t(\tilde{t}_T^a) \mid T \in \mathbf{Thrd}_e\}) \end{cases} \quad \square$$

### Lemma 6.10 (Soundness of ANALYSIS):

Given the sets of valid concrete configurations  $C \in \mathcal{P}(\mathbf{Conf})$  (c.f., Definition 4.4) and abstract configurations  $\tilde{C} \in \mathcal{P}(\mathbf{C\ddot{on}f})$ , such that  $\forall c @ \langle [T, pc_T, \mathfrak{r}_T, t_T^a]_{T \in \mathbf{Thrd}_1}, \mathfrak{x}, \mathbb{I} \rangle \in C : (\forall \langle [T, pc_T^{\tilde{c}}, \tilde{\mathfrak{r}}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_2}, \tilde{\mathfrak{x}}, \tilde{\mathbb{I}} \rangle \in \tilde{C} : (\mathbf{Thrd}_1 = \mathbf{Thrd}_2 = \mathbf{Thrd}) \wedge \exists \tilde{c} \in \tilde{C} : c \in \gamma_{conf}(\tilde{c}) \wedge |\mathbf{Thrd}| < \infty \wedge \forall \tilde{c} @ \langle [T, pc_T^{\tilde{c}}, \tilde{\mathfrak{r}}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{\mathfrak{x}}, \tilde{\mathbb{I}} \rangle \in \tilde{C} : \forall lck \in \mathbf{Lck} : \min(\gamma_t(\mathcal{D}\tilde{\mathbb{L}}(\tilde{\mathbb{I}} lck) = -\infty))$ ), and the times  $t_{io} \in \mathbf{Time}$  and  $\tilde{t}_{io} \in \mathbf{Time}$ , such that  $t_{io} = \max(\gamma_t(\tilde{t}_{io}))$ ,  $(BCET, WCET) @ ANALYSIS(\tilde{C}, \tilde{t}_{io})$  is such that

$$\begin{aligned} \forall c \in C : \forall c' @ \langle [T, pc'_T, \mathfrak{r}'_T, t'^a_T]_{T \in \mathbf{Thrd}}, \mathfrak{x}', \mathbb{I}' \rangle \in \mathbf{Conf} : \\ ((c \xrightarrow{prg} \dots \xrightarrow{prg} c' \wedge \forall T \in \mathbf{Thrd} : STM(T, pc'_T) = [\mathbf{halt}]_{T, pc'_T}) \Rightarrow \\ \forall T \in \mathbf{Thrd} : BCET \leq t'^a_T \leq WCET) \wedge \\ (c \xrightarrow{prg} \dots \xrightarrow{prg} c' \Rightarrow t'^a_T \leq WCET) \end{aligned}$$

given that the algorithm terminates. □

PROOF. Assume that the sets of valid concrete configurations  $C \in \mathcal{P}(\mathbf{Conf})$  (c.f., Definition 4.4) and abstract configurations  $\tilde{C} \in \mathcal{P}(\mathbf{C\ddot{on}f})$  are such that  $\forall c @ \langle [T, pc_T, \mathfrak{r}_T, t_T^a]_{T \in \mathbf{Thrd}_1}, \mathfrak{x}, \mathbb{I} \rangle \in C : (\forall \langle [T, pc_T^{\tilde{c}}, \tilde{\mathfrak{r}}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}_2}, \tilde{\mathfrak{x}}, \tilde{\mathbb{I}} \rangle \in \tilde{C} : (\mathbf{Thrd}_1 = \mathbf{Thrd}_2 = \mathbf{Thrd}) \wedge \exists \tilde{c} \in \tilde{C} : c \in \gamma_{conf}(\tilde{c}) \wedge |\mathbf{Thrd}| < \infty \wedge \forall \tilde{c} @ \langle [T, pc_T^{\tilde{c}}, \tilde{\mathfrak{r}}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{\mathfrak{x}}, \tilde{\mathbb{I}} \rangle \in \tilde{C} : \forall lck \in \mathbf{Lck} : \min(\gamma_t(\mathcal{D}\tilde{\mathbb{L}}(\tilde{\mathbb{I}} lck) = -\infty))$ ), that the times  $t_{io} \in \mathbf{Time}$  and  $\tilde{t}_{io} \in \mathbf{Time}$  are such that  $t_{io} = \max(\gamma_t(\tilde{t}_{io}))$ , and that  $(BCET, WCET) = ANALYSIS(\tilde{C}, \tilde{t}_{io})$ .



Since  $(BCET, WCET) = \text{ANALYSIS}(\tilde{C}, \tilde{t}_{io})$ , it must be that  $(\tilde{C}^f, \tilde{C}^d, \tilde{C}^t) @ \text{ABSEXE}(\tilde{C}, \tilde{t}_{io})$  terminates at some point and that

$$\begin{aligned}
 & \forall c \in C : \forall c' @ \langle [T, pc'_T, r'_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : \\
 & ((c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \wedge \forall T \in \mathbf{Thrd} : \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T}) \Rightarrow \\
 & (\tilde{C}^t \neq \emptyset \vee \\
 & \exists \tilde{c} @ \langle [T, pc_{\tilde{T}}^{\tilde{c}}, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \tilde{C}^f : \forall T \in \mathbf{Thrd} : \\
 & \quad (pc_{\tilde{T}}^{\tilde{c}} = pc'_T \wedge t_T^a \in \gamma_T(\tilde{t}_T^a))) \wedge \\
 & \forall c \in C : \forall c' @ \langle [T, pc'_T, r'_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : \\
 & ((c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \wedge (\text{CYCLE}(\mathbf{Thrd}_{\text{lock}}^{c'}, E^{c'}) \vee \\
 & \quad \exists T \in \mathbf{Thrd} : \exists lck \in \mathbf{Lck} : \\
 & \quad (\text{STM}(T, pc'_T) = [\text{lock } lck]^{pc'_T} \wedge \\
 & \quad \text{OWN}(\mathbb{l}' lck) \notin \{\perp_{\text{thrd}}, T\} \wedge \\
 & \quad \text{STM}(\text{OWN}(\mathbb{l}' lck), pc'_{\text{OWN}(\mathbb{l}' lck)}) = \\
 & \quad \quad [\text{halt}]^{pc'_{\text{OWN}(\mathbb{l}' lck)}))) \Rightarrow \\
 & (\tilde{C}^t \neq \emptyset \vee \tilde{C}^d \neq \emptyset))
 \end{aligned}$$

(Lemma 6.8). It is thus apparent that if  $\tilde{C}^d \cup \tilde{C}^t \neq \emptyset$ , there might exist an infinite transition sequence in the concrete case. However, it is easy to see that (as returned by the algorithm)  $-\infty$  is a safe approximation of the BCET and that  $\infty$  is a safe approximation of the WCET for all such (and all other) cases.

If  $\tilde{C}^d \cup \tilde{C}^t = \emptyset$ , then all concrete transition sequences are of finite length and  $\forall c \in C : \forall c' @ \langle [T, pc'_T, r'_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : ((c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \wedge \forall T \in \mathbf{Thrd} : \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T}) \Rightarrow \exists \langle [T, pc_{\tilde{T}}^{\tilde{c}}, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{\mathbb{x}}, \tilde{\mathbb{l}} \rangle \in \tilde{C}^f : (pc_{\tilde{T}}^{\tilde{c}} = pc'_T \wedge t_T^a \in \gamma_T(\tilde{t}_T^a)))$  (Lemma 6.8). Thus, since the structure of the algorithm trivially gives that the smallest possible estimation of the BCET,  $BCET$ , and the largest possible estimation of the WCET,  $WCET$ , among the derived final abstract configurations in  $\tilde{C}^f$  are found (c.f., Definition 6.9), it must be that  $\forall c \in C : \forall c' @ \langle [T, pc'_T, r'_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : ((c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \wedge \forall T \in \mathbf{Thrd} : \text{STM}(T, pc'_T) = [\text{halt}]^{pc'_T}) \Rightarrow \forall T \in \mathbf{Thrd} : BCET \leq t_T^a \leq WCET)$ . But, then it must also be that  $\forall c \in C : \forall c' @ \langle [T, pc'_T, r'_T, t_T^a]_{T \in \mathbf{Thrd}}, \mathbb{x}', \mathbb{l}' \rangle \in \mathbf{Conf} : (c \xrightarrow{\text{prg}} \dots \xrightarrow{\text{prg}} c' \Rightarrow \forall T \in \mathbf{Thrd} : t_T^a \leq WCET)$  since time only moves forward (c.f., Assumption 5.50), which concludes the proof. ■



# Chapter 7

## Examples

To clarify and explain the analysis defined in Chapters 5 and 6, this chapter instantiates it for some example PPL programs.

### 7.1 Communication

This case shows the recursive behavior of ABSEXE; i.e., how it peeks into the future to derive safe write histories for unsafe load-statements.

For the program,  $\mathbf{Thrd} = \{T_1, T_2, T_3\}$ , defined in Table 7.1, it is easy to see that  $\mathbf{Reg}_{T_1} = \{r\}$ ,  $\mathbf{Reg}_{T_2} = \{r\}$ ,  $\mathbf{Reg}_{T_3} = \{r\}$ ,  $\mathbf{Var} = \{x, y, z\}$  and  $\mathbf{Lck} = \emptyset$ . Note that  $r$  represents local memory within each thread; i.e., the register-name  $r$  can refer to three different memory locations – what location it refers to depends on which thread is considered.

Assume that  $\text{ABSTIME}(\tilde{c}, T)$ , where  $\tilde{c} @ \langle [T, pc_T, \tilde{r}_T, \tilde{r}_T^a]_{T \in \mathbf{Thrd}_e}, \tilde{x}, \tilde{l} \rangle \in$

$T_1 @ (1, [\text{load } r \text{ from } x]^1; [\text{store } r \text{ to } y]^2; [\text{halt}]^3)$
$T_2 @ (2, [\text{load } r \text{ from } y]^1; [\text{store } r \text{ to } z]^2; [\text{halt}]^3)$
$T_3 @ (3, [\text{if } r \leq 3 \text{ goto } 4]^1; [\text{store } r \text{ to } x]^2; [\text{skip}]^3; [\text{halt}]^4)$

Table 7.1: Communicating threads – Program.

$\mathbf{Conf}$  and  $T \in \mathbf{Thrd}_{\tilde{c}}$ , is such that for any  $\tilde{c}$ , it assumes the values described by the below table.

$pc_T$	$T_1$	$T_2$	$T_3$
1	[1,5]	[2,6]	[1,4]
2	[1,3]	[2,3]	[3,4]
3	—	—	[3,3]

Also assume that  $\tilde{c}_0^0 @ \langle [T, pc_T, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{l} \rangle$  is as described in Table 7.2. (Due to the semantics of the program, the parts of the states that are left out from the table are of no interest for this case study.)

Tables 7.2 and 7.3 collect all the configurations derived by  $\text{ABSEXE}(\{\tilde{c}_0^0\}, [-\infty, \infty])$  during the analysis described by  $\text{ANALYSIS}(\{\tilde{c}_0^0\}, [-\infty, \infty])$ . A ‘—’ indicates that the entry is not applicable to (i.e., not included in) the configuration. Figure 7.4 shows the order in which the configurations are derived; i.e., the relation between the derived configurations. In the figure, final configurations are circled and timed-out configurations are circled and marked with a ‘t’. To see how new recursive instances of  $\text{ABSEXE}$  are created, note that when  $\mathbf{Thrd}_{\tilde{c}} = \{T_1, T_2, T_3\}$ , then  $\mathbf{Var}_{\mathbf{g}} = \{x, y\}$ ; when  $\mathbf{Thrd}_{\tilde{c}} = \{T_1, T_3\}$ , then  $\mathbf{Var}_{\mathbf{g}} = \{x\}$ ; and when  $\mathbf{Thrd}_{\tilde{c}} = \{T_2, T_3\}$ , then  $\mathbf{Var}_{\mathbf{g}} = \emptyset$ .

It is apparent that  $\text{ABSEXE}(\{\tilde{c}_0^0\}, [-\infty, \infty]) = (\{\tilde{c}_{11}^0, \tilde{c}_{23}^0\}, \emptyset, \emptyset)$ ; i.e.,  $\tilde{c}_{11}^0$  and  $\tilde{c}_{23}^0$  are final-state configurations and there are no deadlocked or timed-out configurations. According to Algorithm 6.13, it is thus easy to see that the estimated timing bounds are:

$$\left\{ \begin{array}{l} BCET = \min(\{\max(\{\min(\gamma_i(\tilde{t}_T^a) \mid T \in \mathbf{Thrd}\}) \mid \\ \langle [T, pc_T, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{l} \rangle \in \{\tilde{c}_{11}^0, \tilde{c}_{23}^0\}\}) = 4 \\ WCET = \max(\{\max(\{\max(\gamma_i(\tilde{t}_T^a) \mid T \in \mathbf{Thrd}\}) \mid \\ \langle [T, pc_T, \tilde{r}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{l} \rangle \in \{\tilde{c}_{11}^0, \tilde{c}_{23}^0\}\}) = 11 \end{array} \right.$$

$\tilde{c}$	$pc_{T_1}$	$pc_{T_2}$	$pc_{T_3}$	$\tilde{r}_{T_1}$	$\tilde{r}_{T_2}$	$\tilde{r}_{T_3}$	$\tilde{r}_{T_1}^a$	$\tilde{r}_{T_2}^a$	$\tilde{r}_{T_3}^a$	$(\tilde{x} \ x) \ T_3$	$(\tilde{x} \ y) \ T_1$	$(\tilde{x} \ z) \ T_2$
$\tilde{c}_0^0$	1	1	1	[0,0]	[0,0]	[2,4]	[0,0]	[0,0]	[0,0]	{([1,1],[0,0])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ )}
$\tilde{c}_0^{11}$	–	1	1	–	[0,0]	[2,4]	–	[0,0]	[0,0]	{([1,1],[0,0])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ )}
$\tilde{c}_{11}^{11}$	–	2	4	–	[5,5]	[2,3]	–	[2,6]	[1,4]	{([1,1],[0,0])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ )}
$\tilde{c}_{12}^{11}$	–	3	4	–	[5,5]	[2,3]	–	[4,9]	[1,4]	{([1,1],[0,0])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ ), ([5,5],[4,9])}
$\tilde{c}_{21}^{11}$	–	2	2	–	[5,5]	[4,4]	–	[2,6]	[1,4]	{([1,1],[0,0])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ )}
$\tilde{c}_{22}^{11}$	–	3	3	–	[5,5]	[4,4]	–	[4,9]	[4,8]	{([1,1],[0,0]), ([4,4],[4,8])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ ), ([5,5],[4,9])}
$\tilde{c}_0^{12}$	1	–	1	[0,0]	–	[2,4]	[0,0]	–	[0,0]	{([1,1],[0,0])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ )}
$\tilde{c}_0^{22}$	–	–	1	–	–	[2,4]	–	–	[0,0]	{([1,1],[0,0])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ )}
$\tilde{c}_{11}^{22}$	–	–	4	–	–	[2,3]	–	–	[1,4]	{([1,1],[0,0])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ )}
$\tilde{c}_{21}^{22}$	–	–	2	–	–	[4,4]	–	–	[1,4]	{([1,1],[0,0])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ )}
$\tilde{c}_{22}^{22}$	–	–	3	–	–	[4,4]	–	–	[4,8]	{([1,1],[0,0]), ([4,4],[4,8])}	{([5,5],[0,0])}	{( $\tilde{\perp}_{val}$ , $\tilde{\perp}_t$ )}
$\tilde{c}$	$pc_{T_1}$	$pc_{T_2}$	$pc_{T_3}$	$\tilde{r}_{T_1}$	$\tilde{r}_{T_2}$	$\tilde{r}_{T_3}$	$\tilde{r}_{T_1}^a$	$\tilde{r}_{T_2}^a$	$\tilde{r}_{T_3}^a$	$(\tilde{x} \ x) \ T_3$	$(\tilde{x} \ y) \ T_1$	$(\tilde{x} \ z) \ T_2$

Table 7.2: Communicating threads – Configurations (First half).

$\tilde{c}$	$pc_{T_1}$	$pc_{T_2}$	$pc_{T_3}$	$\tilde{r}_{T_1}$	$\tilde{r}_{T_2}$	$\tilde{r}_{T_3}$	$\tilde{r}_{T_1}^a$	$\tilde{r}_{T_2}^a$	$\tilde{r}_{T_3}^a$	$(\tilde{x} \ x) T_3$	$(\tilde{x} \ y) T_1$	$(\tilde{x} \ z) T_2$
$\tilde{c}_1^{12}$	2	–	1	[1, 4]	–	[2, 4]	[1, 5]	–	[0, 0]	{([1, 1], [0, 0])}	{([5, 5], [0, 0])}	{( $\tilde{I}_{val}$ , $\tilde{I}_t$ )}
$\tilde{c}_{11}^{12}$	3	–	4	[1, 4]	–	[2, 3]	[2, 8]	–	[1, 4]	{([1, 1], [0, 0])}	{([5, 5], [0, 0]), ([1, 4], [2, 8])}	{( $\tilde{I}_{val}$ , $\tilde{I}_t$ )}
$\tilde{c}_{21}^{12}$	3	–	2	[1, 4]	–	[4, 4]	[2, 8]	–	[1, 4]	{([1, 1], [0, 0])}	{([5, 5], [0, 0]), ([1, 4], [2, 8])}	{( $\tilde{I}_{val}$ , $\tilde{I}_t$ )}
$\tilde{c}_{22}^{12}$	3	–	3	[1, 4]	–	[4, 4]	[2, 8]	–	[4, 8]	{([1, 1], [0, 0]), ([4, 4], [4, 8])}	{([5, 5], [0, 0]), ([1, 4], [2, 8])}	{( $\tilde{I}_{val}$ , $\tilde{I}_t$ )}
$\tilde{c}_1^0$	2	2	1	[1, 4]	[1, 5]	[2, 4]	[1, 5]	[2, 6]	[0, 0]	{([1, 1], [0, 0])}	{([5, 5], [0, 0])}	{( $\tilde{I}_{val}$ , $\tilde{I}_t$ )}
$\tilde{c}_{11}^0$	3	3	4	[1, 4]	[1, 5]	[2, 3]	[2, 8]	[4, 9]	[1, 4]	{([1, 1], [0, 0])}	{([5, 5], [0, 0]), ([1, 4], [2, 8])}	{( $\tilde{I}_{val}$ , $\tilde{I}_t$ ), ([1, 5], [4, 9])}
$\tilde{c}_{21}^0$	3	3	2	[1, 4]	[1, 5]	[4, 4]	[2, 8]	[4, 9]	[1, 4]	{([1, 1], [0, 0])}	{([5, 5], [0, 0]), ([1, 4], [2, 8])}	{( $\tilde{I}_{val}$ , $\tilde{I}_t$ ), ([1, 5], [4, 9])}
$\tilde{c}_{22}^0$	3	3	3	[1, 4]	[1, 5]	[4, 4]	[2, 8]	[4, 9]	[4, 8]	{([1, 1], [0, 0]), ([4, 4], [4, 8])}	{([5, 5], [0, 0]), ([1, 4], [2, 8])}	{( $\tilde{I}_{val}$ , $\tilde{I}_t$ ), ([1, 5], [4, 9])}
$\tilde{c}_{23}^0$	3	3	4	[1, 4]	[1, 5]	[4, 4]	[2, 8]	[4, 9]	[7, 11]	{([1, 1], [0, 0]), ([4, 4], [4, 8])}	{([5, 5], [0, 0]), ([1, 4], [2, 8])}	{( $\tilde{I}_{val}$ , $\tilde{I}_t$ ), ([1, 5], [4, 9])}
$\tilde{c}$	$pc_{T_1}$	$pc_{T_2}$	$pc_{T_3}$	$\tilde{r}_{T_1}$	$\tilde{r}_{T_2}$	$\tilde{r}_{T_3}$	$\tilde{r}_{T_1}^a$	$\tilde{r}_{T_2}^a$	$\tilde{r}_{T_3}^a$	$(\tilde{x} \ x) T_3$	$(\tilde{x} \ y) T_1$	$(\tilde{x} \ z) T_2$

Table 7.3: Communicating threads – Configurations (Second half).

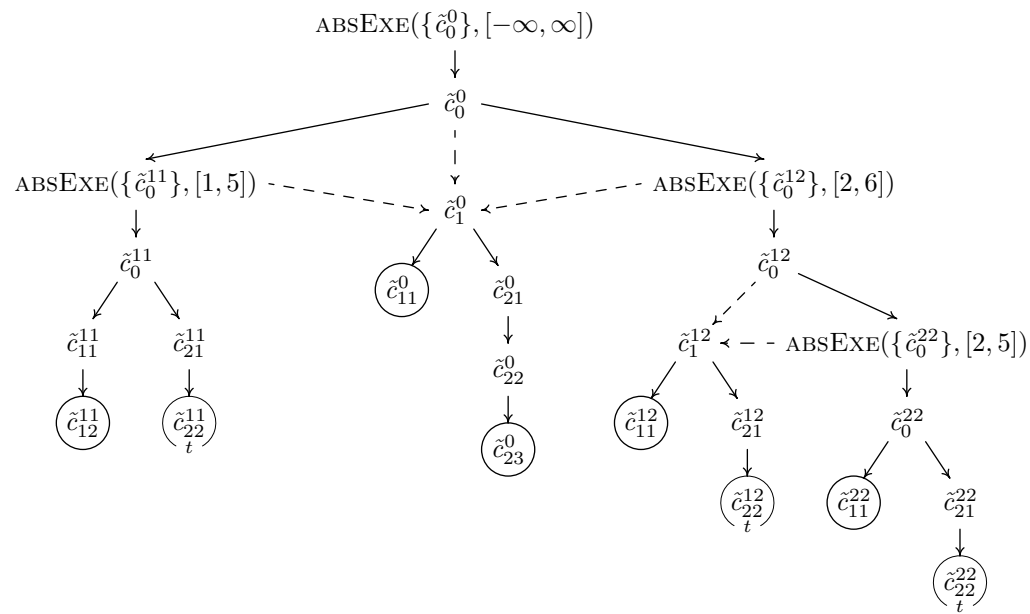


Figure 7.4: Communicating threads – Configuration relations.

$T_1 @ (1, [\text{lock } 1a]^1; [\text{lock } 1b]^2; [\text{unlock } 1a]^3; [\text{unlock } 1b]^4; [\text{halt}]^5)$ $T_2 @ (2, [\text{lock } 1a]^1; [\text{lock } 1b]^2; [\text{halt}]^3)$
---

Table 7.5: Synchronization (Deadlock) – Program.

## 7.2 Synchronization – Deadlocks

This case shows how ABSEXE identifies deadlocked configurations and how it discontinues deadlocked configurations that lack concrete counterparts.

For the program,  $\mathbf{Thrd} = \{T_1, T_2\}$ , defined in Table 7.5, it is easy to see that  $\mathbf{Reg}_{T_1} = \emptyset$ ,  $\mathbf{Reg}_{T_2} = \emptyset$ ,  $\mathbf{Var} = \emptyset$  and  $\mathbf{Lck} = \{1a, 1b\}$ . Assume that  $\text{ABSTIME}(\tilde{c}, T)$ , where  $\tilde{c} @ \langle [T, pc_T, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{t} \rangle \in \mathbf{C\o{on}f}$  and  $T \in \mathbf{Thrd}$ , is such that for any  $\tilde{c}$ , it assumes the values described by the below table.

$pc_T$	$T_1$	$T_2$
1	[2, 2]	[1, 2]
2	[1, 2]	[1, 2]
3	[1, 1]	–
4	[1, 1]	–

Also assume that  $\tilde{c}_0^0 @ \langle [T, pc_T, \tilde{x}_T, \tilde{t}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{t} \rangle$  is as described in Table 7.6. (Due to the semantics of the program, the parts of the states that are left out from the table are of no interest for this case study.)

Table 7.6 collects all the configurations derived by  $\text{ABSEXE}(\{\tilde{c}_0^0\}, [-\infty, \infty])$  during the analysis described by  $\text{ANALYSIS}(\{\tilde{c}_0^0\}, [-\infty, \infty])$ . Figure 7.7 shows the order in which the configurations are derived; i.e., the relation between the derived configurations. In the figure, final configurations are circled, deadlocked configurations are circled and marked with a ‘d’ and discontinued configurations are crossed out. Note that  $\tilde{c}_2^4$  occurs since  $T_2$  has been waiting to acquire 1a and is now assigned it, which means that  $T_2$ ’s accumulated execution time will be advanced to simulate the spin-lock waiting of the concrete semantics (c.f., the discussion in the proof of Lemma 5.57).

It is apparent that  $\text{ABSEXE}(\{\tilde{c}_0^0\}, [-\infty, \infty]) = (\{\tilde{c}_2^7\}, \{\tilde{c}_4^2\}, \emptyset)$ ; i.e.,  $\tilde{c}_2^7$  is a final-state configuration,  $\tilde{c}_4^2$  is a deadlocked configuration, and there are no timed-out configurations.



$\tilde{c}$	$pc_{T_1}$	$pc_{T_2}$	$\tilde{t}_{T_1}^a$	$\tilde{t}_{T_2}^a$	$\tilde{\mathbb{I}} \text{ 1a}$	$\tilde{\mathbb{I}} \text{ 1b}$
$\tilde{c}_0^0$	1	1	[0, 0]	[0, 0]	( <i>unlocked</i> , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )	( <i>unlocked</i> , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}_1^1$	2	1	[2, 2]	[0, 0]	( <i>locked</i> , $T_1$ , $[-\infty, 2]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )	( <i>unlocked</i> , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}_1^2$	2	1	[2, 2]	[0, 0]	( <i>locked</i> , $T_1$ , $[-\infty, 2]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )	( <i>unlocked</i> , $T_2$ , $[-\infty, 4]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}_2^2$	3	1	[3, 4]	[0, 0]	( <i>locked</i> , $T_1$ , $[-\infty, 2]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )	( <i>locked</i> , $T_1$ , $[-\infty, 4]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}_1^3$	4	1	[4, 5]	[0, 0]	( <i>unlocked</i> , $\perp_{thrd}$ , $[-\infty, 2]$ , $T_1$ , [4, 5])	( <i>locked</i> , $T_1$ , $[-\infty, 4]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}_1^4$	5	1	[5, 6]	[0, 0]	( <i>unlocked</i> , $T_1$ , $[-\infty, 12]$ , $T_1$ , [4, 5])	( <i>unlocked</i> , $\perp_{thrd}$ , $[-\infty, 4]$ , $T_1$ , [5, 6])
$\tilde{c}_4^2$	4	1	[4, 5]	[1, 2]	( <i>unlocked</i> , $T_2$ , $[-\infty, 12]$ , $T_1$ , [4, 5])	( <i>locked</i> , $T_1$ , $[-\infty, 4]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}_1^5$	4	2	[4, 5]	[4, 12]	( <i>locked</i> , $T_2$ , $[-\infty, 12]$ , $T_1$ , [4, 5])	( <i>locked</i> , $T_1$ , $[-\infty, 4]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}_1^6$	5	2	[5, 6]	[4, 12]	( <i>locked</i> , $T_2$ , $[-\infty, 12]$ , $T_1$ , [4, 5])	( <i>unlocked</i> , $\perp_{thrd}$ , $[-\infty, 4]$ , $T_1$ , [5, 6])
$\tilde{c}_1^7$	5	2	[5, 6]	[4, 12]	( <i>locked</i> , $T_2$ , $[-\infty, 12]$ , $T_1$ , [4, 5])	( <i>unlocked</i> , $T_1$ , $[-\infty, 18]$ , $T_1$ , [5, 6])
$\tilde{c}_2^7$	5	3	[5, 6]	[5, 18]	( <i>locked</i> , $T_2$ , $[-\infty, 12]$ , $T_1$ , [4, 5])	( <i>locked</i> , $T_2$ , $[-\infty, 18]$ , $T_1$ , [5, 6])
$\tilde{c}_2^1$	1	2	[0, 0]	[1, 2]	( <i>locked</i> , $T_2$ , $[-\infty, 2]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )	( <i>unlocked</i> , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}_3^2$	1	2	[0, 0]	[1, 2]	( <i>locked</i> , $T_2$ , $[-\infty, 2]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )	( <i>unlocked</i> , $T_1$ , $[-\infty, 4]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}_4^2$	1	3	[0, 0]	[2, 4]	( <i>locked</i> , $T_2$ , $[-\infty, 2]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )	( <i>locked</i> , $T_2$ , $[-\infty, 4]$ , $\perp_{thrd}$ , $\tilde{\mathbb{I}}_t$ )
$\tilde{c}$	$pc_{T_1}$	$pc_{T_2}$	$\tilde{t}_{T_1}^a$	$\tilde{t}_{T_2}^a$	$\tilde{\mathbb{I}} \text{ 1a}$	$\tilde{\mathbb{I}} \text{ 1b}$

Table 7.6: Synchronization (Deadlock) – Configurations.

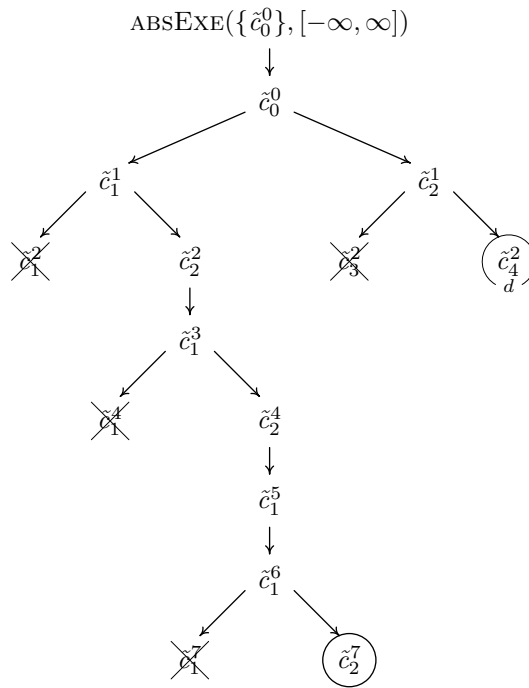


Figure 7.7: Synchronization (Deadlock) – Configuration relations.

According to Algorithm 6.13, it is thus easy to see that the estimated timing bounds are:

$$\begin{cases} BCET = -\infty \\ WCET = \infty \end{cases}$$

$T_1 @ (1, [\text{lock } 1]^1; [\text{halt}]^2)$ $T_2 @ (2, [\text{lock } 1]^1; [\text{halt}]^2)$
--

Table 7.8: Synchronization (Deadline miss) – Program.

### 7.3 Synchronization – Deadline Miss

This case illustrates how the analysis discontinues configurations for which an assigned lock owner does not acquire the lock in time. It also illustrates how the analysis detects deadlocks.

For the program,  $\mathbf{Thrd} = \{T_1, T_2\}$ , defined in Table 7.8, it is easy to see that  $\mathbf{Reg}_{T_1} = \emptyset$ ,  $\mathbf{Reg}_{T_2} = \emptyset$ ,  $\mathbf{Var} = \emptyset$  and  $\mathbf{Lck} = \{1\}$ . Assume that  $\text{ABSTIME}(\tilde{c}, T)$ , where  $\tilde{c} @ \langle [T, pc_T, \tilde{r}_T, \tilde{r}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{I} \rangle \in \mathbf{C\o n f}$  and  $T \in \mathbf{Thrd}$ , is such that for any  $\tilde{c}$ , it assumes the values described by the below table.

$pc_T$	$T_1$	$T_2$
1	[5, 5]	[10, 10]

Also assume that  $\tilde{c}_0 @ \langle [T, pc_T, \tilde{r}_T, \tilde{r}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{I} \rangle$  is as described in Table 7.9. (Due to the semantics of the program, the parts of the states that are left out from the table are of no interest for this case study.)

Table 7.9 collects all the configurations derived by  $\text{ABSEXE}(\{\tilde{c}_0\}, [-\infty, \infty])$  during the analysis described by  $\text{ANALYSIS}(\{\tilde{c}_0\}, [-\infty, \infty])$ . Figure 7.10 shows the order in which the configurations are derived; i.e., the relation between the derived configurations. In the figure, deadlocked configurations are circled and marked with a ‘d’ and discontinued configurations are crossed out. It is apparent that  $\text{ABSEXE}(\{\tilde{c}_0\}, [-\infty, \infty]) = (\emptyset, \{\tilde{c}_1\}, \emptyset)$ ; i.e., there are no final-state or timed-out configurations, and  $\tilde{c}_1$  is a deadlocked configuration. According to Algorithm 6.13, it is thus easy to see that the estimated timing bounds are:

$$\begin{cases} BCET = -\infty \\ WCET = \infty \end{cases}$$

$\tilde{c}$	$pc_{T_1}$	$pc_{T_2}$	$\tilde{t}_{T_1}^a$	$\tilde{t}_{T_2}^a$	$\tilde{I} \ 1$
$\tilde{c}_0$	1	1	[0, 0]	[0, 0]	( <i>unlocked</i> , $\perp_{thrd}$ , $\tilde{I}_t$ , $\perp_{thrd}$ , $\tilde{I}_t$ )
$\tilde{c}_1$	2	1	[5, 5]	[0, 0]	( <i>locked</i> , $T_1$ , $[-\infty, 5]$ , $\perp_{thrd}$ , $\tilde{I}_t$ )
$\tilde{c}_2$	1	1	[0, 0]	[10, 10]	( <i>unlocked</i> , $T_2$ , $[-\infty, 5]$ , $\perp_{thrd}$ , $\tilde{I}_t$ )
$\tilde{c}$	$pc_{T_1}$	$pc_{T_2}$	$\tilde{t}_{T_1}^a$	$\tilde{t}_{T_2}^a$	$\tilde{I} \ 1$

Table 7.9: Synchronization (Deadline miss) – Configurations.

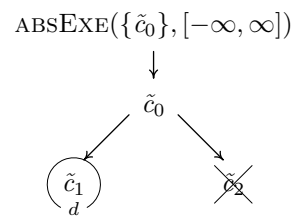


Figure 7.10: Synchronization (Deadline miss) – Configuration relations.

## Chapter 8

# Conclusions

In this chapter, some distinguishing properties of the defined analysis will be discussed. Feedback on the Research Questions and issues to be further considered and investigated will also be given.

### 8.1 The Underlying Architecture

The analysis is defined for an arbitrary underlying architecture (that is, however, restricted to the constraints in Assumptions 4.1 and 4.3). The actual underlying system could be an operating system as well as raw hardware as long as both thread-private and globally shared memory, and some form of synchronization primitive, correlating to the description given in the beginning of Chapter 4 is provided. The assumed architecture should be fairly realistic since any mature operating system and any common (single- or multi-core) CPU provides the described features at some abstraction level. For example, any Real-Time operating system should provide spin-locks for thread synchronization and any CPU instruction set should provide the ability to lock the system bus to provide atomic execution of a set of machine operations (since one single instruction of the instruction set often is mapped to a set of machine instructions).

The `lock-` and `unlock-` statements could be used to model the `LOCK` prefix in the x86 instruction set. This prefix is used for asserting atomic execution of an instruction [41, 81]. The `lock-` and `unlock-` statements also trivially correspond to higher level spin-locking primitives, such as those provided by

the POSIX thread library [10, 39].

Many of the principles applied in the analysis presented in Chapters 5 and 6 to solve the problems arising from abstracting time using intervals are also applicable to analysis of systems with distributed address spaces. If considering processes on one and the same CPU, then communication between these processes is often implemented using a memory buffer which is then to be considered as shared memory. This means that the same principles as those presented in this thesis would be applicable to such an analysis. If communication is performed using, for example, message passing and “Any”-communication is available (i.e., several processes could send a message to a given receiving process and/or several processes could receive a message sent from a given process), this would also require some form of prediction of what values could be transferred between processes.

The necessity of allowing  $\text{TIME}(c, T) = 0$  for some configuration,  $c \in \mathbf{Conf}$ , and thread,  $T \in \mathbf{Thrd}$ , is apparent when considering the following case. If mutual exclusion is inherent in some instruction of the modeled instruction set, for example, `store`, then the `lock`- and `unlock`-statements could be regarded as macros without timing that should encapsulate all `store`-statements in a program.

PPL is designed to bring the focus of the analysis to thread synchronization and global data flow. The method presented in this thesis might have to be extended in order to cover all the aspects of a real instruction set, such as those of for example the ARM or PowerPC architectures [5, 42]. This will be further investigated.

If limiting the register (and variable) sizes the architecture would become more realistic. However, wrap-around effects could render loops non-terminating in the abstract case even if this would not concretely occur. See Section 8.3 for a discussion on more non-terminating cases.

## 8.2 Algorithmic Structure & Complexity

The analysis presented in Chapters 5 and 6 is based on synchronously advancing the threads of a program between their respective program points while keeping the threads fairly synchronized in time (c.f., Algorithm 6.1 and Tables 5.5 and 5.6). The advantage of this approach (i.e., abstracting time using intervals) in conjunction with the defined domain for variable states (c.f., Section 5.5) is that a relatively high precision is achieved. And, when  $|\mathbf{Thrd}| = 1$ , the analysis result will be equivalent to that of the corresponding sequential ana-

lysis (c.f., [28]). Another advantage is that the time-complexity of the analysis is more dependent on the number of program points in each thread than on the timing behavior of the program, compared to stepping through strict timing events, like in the concrete semantics.

Keeping the threads fairly synchronized in the analysis is also an advantage when considering its memory-complexity. Keeping the threads synchronized means that the write history for any thread on any variable will always be as small as possible since writes become outdated after a minimal amount of steps in the analysis and are then trimmed away from the history. In other words, the write history for any thread on any variable will never be larger than absolutely necessary.

One of the main disadvantages with keeping write history for each thread on each variable (which is expected to be necessary in order to keep the over-approximations at a reasonable level) is that the history must be trimmed. Trimming is an advantage for the memory-complexity as discussed above, but could be a serious disadvantage for the time-complexity if the analyzed program consists of many variables and many write-intensive threads.

The definition of the abstract state for locks contains some concrete parts (e.g., the owners of the locks). This is necessary since too much precision would be lost, and the timing approximations would become useless (i.e., too over-approximate), otherwise. However, this is very bad from a complexity point of view. The result of not abstracting some parts of a state is that (at least) all the concrete counterparts must be evaluated. Any reasonably precise abstractions of the parts of the lock states that are currently kept concrete have not been found. In case of serious complexity issues (which are very likely to occur), candidate domains for such abstractions must be further investigated.

It should be apparent that a given (abstract) configuration could result in two or more configurations for each thread issuing an `if`- or a `lock`-statement in a transition (c.f., Tables 5.5 and 5.6). Merging of configurations could be performed to reduce the complexity of the analysis. Using the Control Flow Graph (CFG) of the program, suitable merge-points within each thread can be found [25]. Typically, such points have multiple incoming edges. However, even if adding merging to the analysis, it will most probably happen very infrequently (if ever at all). This is since all the concrete parts (i.e., the program counters, lock owners, etc.) must be equal between the configurations to merge. As discussed above, domains for abstraction of the concrete parts of the configuration might have to be further investigated in case of serious complexity issues. Abstracting more parts of the configurations would also increase the possibility that merging could be more frequently performed. Although, the

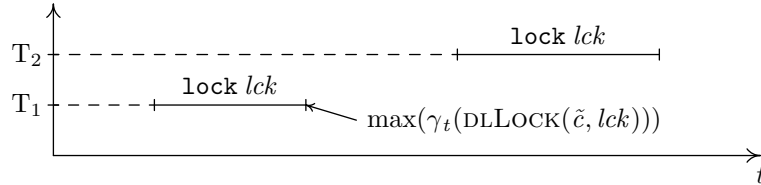


Figure 8.1: Lock owner assignments based on  $\tilde{c} \in \mathbf{Conf}$  resulting in one valid and one invalid configuration.

derived timing approximations could become very pessimistic.

It is very important to note that several configurations that lack valid concrete counterparts (c.f., Definition 4.4) are added to the work-list for several situations. One such situation is when one sole thread issues `lock lck` for some free lock,  $lck \in \mathbf{Lck}$ , in a transition. A unique transition (i.e., resulting configuration) is possible for each thread that might issue `lock lck` somewhere in the program. A new configuration for each such thread, where the given thread is the new owner of  $lck$ , will thus be derived. Consider the situation depicted in Figure 8.1 (c.f., the case study in Section 7.3).  $T_1$  is obviously the thread issuing `lock lck` first in any considered case. However, two new configurations are derived on the transition; one where  $T_1$  is the new owner of  $lck$  and one where  $T_2$  is the new owner of  $lck$ . Obviously, only the configuration for which  $T_1$  is the owner of  $lck$  has valid concrete counterparts since  $T_2$  will not acquire  $lck$  before some other thread (i.e.,  $T_1$ ) is guaranteed to have acquired  $lck$ . Thus, the case that  $T_2$  is the new owner of  $lck$  will be discontinued since the lock is not acquired by  $T_2$  before the deadline expires (c.f., Algorithm 6.6).

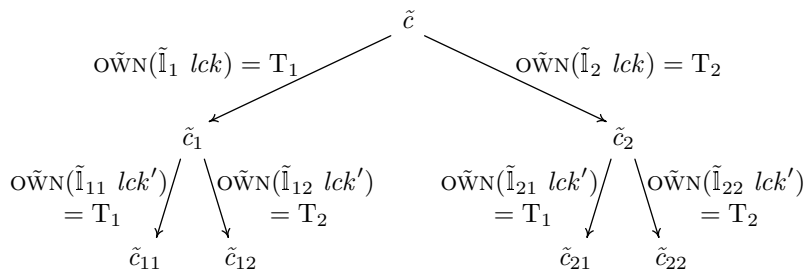
Another such situation will result for the program described in Figure 8.2a, assuming that the timing of the first `lock`-statement in the two threads overlap (c.f., the case study in Section 7.2). (Note that the given code is guaranteed not to deadlock, provided that both threads eventually release the two locks again.) Assume that the program is described by  $\tilde{c} @ \langle [T, pc_T, \tilde{\pi}_T, \tilde{\gamma}_T^a]_{T \in \mathbf{Thrd}}, \tilde{x}, \tilde{\mathbb{I}} \rangle \in \mathbf{Conf}$  and that  $pc_{T_1} = pc_{T_2} = 1$ . The resulting lock-owner assignments (i.e., configurations) are given in Figure 8.2b. Obviously, only  $\tilde{c}_{11}$  and  $\tilde{c}_{22}$  have valid concrete counterparts.  $\tilde{c}_{12}$  and  $\tilde{c}_{21}$  will be discontinued (i.e., removed from the work-list) since there is a cycle in the dependency graph containing at least one lock (here, that lock is  $lck'$ ) that has the state *unlocked* (c.f., Algorithm 6.6). If  $\tilde{c}_{12}$  and  $\tilde{c}_{21}$  were not discontinued, the analysis would itself deadlock.

It is easy to see that all these complexity hazards really explode when com-



$$T_1 : [\text{lock } lck]^1; [\text{lock } lck']^2; \dots$$

$$T_2 : [\text{lock } lck]^1; [\text{lock } lck']^2; \dots$$

 (a) The program described by  $\tilde{c}$ .


(b) Resulting configurations.

Figure 8.2: Lock owner assignments based on  $\tilde{c} \in \mathbf{Conf}$  resulting in two valid and two invalid (i.e., falsely deadlocked) configurations.

bined (e.g., when they occur in different threads for a single transition). This could render the analysis extremely complex. A good thing to notice, though, is that a well structured parallel program will be less complex to analyze [53]. The threads in a well structured program typically work as much as possible on local data and do not synchronize more than is absolutely necessary.

Another good thing to notice is that the complexity is lowered by keeping a high precision in the calculation of the accumulated execution time for threads issuing lock-statements. Since  $\mathbf{Time} = \mathbf{Intv}$ , a high precision in this calculation will give a narrow accumulated execution time. This will lead to that a minimum number of states need to be explored since the timing of individual threads will not overlap more than necessary. Of course, this part of the complexity is also dependent on the precision of  $\mathbf{ABSTIME}$ ; i.e., the accuracy in the model of the underlying architecture.

### 8.3 Non-terminating Transition Sequences

As previously discussed,  $\mathbf{ISDEADLOCK}$  catches some configurations that will never reach the final state (c.f., Algorithm 6.4). However, it is not guaranteed to identify all such configurations. This means that the analysis could actually deadlock for some cases that  $\mathbf{ISDEADLOCK}$  misses to identify as never reach-

ing the final state. The corresponding can be said if ISVALID wrongly identifies a configuration as valid (c.f., Algorithm 6.6).

Infinite loops are recognized by ISTIMEOUT( $\tilde{c}, \tilde{t}_{to}$ ), given that time moves forward and the timeout is finite; i.e., it cannot be that  $0 \in \text{ABSTIME}(\tilde{c}', T)$  for all  $\tilde{c}' \in \mathbf{C\tilde{o}nf}$  occurring in the loop in  $T$  and  $\max(\gamma_t(\tilde{t}_{to})) = \infty$ . If ABSTIME includes 0 for all statements of an infinite loop in some thread, then the algorithm will not terminate.

To avoid part of this problem, another timeout variable could be added to the analysis. This timeout could be used to identify that the upper bound of a single thread's accumulated execution time has reached a limit. However, this does not resolve the case that, for all  $\tilde{c}' \in \mathbf{C\tilde{o}nf}$  in the loop,  $\text{ABSTIME}(\tilde{c}', T) = [0, 0]$ .

To address this case, a transition counter could be used. There could be one counter for each thread individually and/or one counter for all threads combined. The counter(s) could either count all transitions or only transitions that are consecutively done in  $[0, 0]$  amount of time, depending on whether a second timeout is used. When the counter reaches a specific limit, the configuration could be considered to be timed out, which means that the corresponding transition sequence could be of infinite length.

Even if all concrete transition sequences given some initial configuration terminate, all abstract transition sequences resulting from the corresponding abstract initial configuration are not guaranteed to terminate. This is due to over-approximations inherent in the abstract interpretation of the PPL semantics. Thus, all the complications discussed above can occur in the abstract case even if they do not in the concrete case.

## 8.4 The Research Questions

**Question 1:** *“What are the distinguishing features of a parallel computer system (i.e., the hardware and software combination) that must be taken into account in a timing analysis on the code level?”*

The most important aspects found are some means of communication and synchronization between the parallel entities. In this thesis, only the software (i.e., code) level is considered: shared memory is used to represent the communication medium; locks that can be acquired in a mutually exclusive manner using spin-locking are used to represent the synchronization medium; and threads are used to represent the parallel entities.

**Question 2:** “How can a parallel computer system be analyzed to derive safe and tight estimations on its timing bounds?”

It has been shown that Abstract Interpretation is a suitable technique for deriving safe timing bound estimates for a given program and timing model. The resulting tightness of the estimates depends both on the precision of the used abstract domains, the precision of the timing analysis itself and the precision of the timing model. Further evaluation, preferably based on an implementation of the analysis, must be performed before the tightness of the approach used in this thesis can be commented upon.

**Question 3:** “How can analysis termination be guaranteed?”

Some techniques to increase the termination-probability have been already incorporated into the analysis and were discussed in the previous sections; one such technique is the discontinuation of configurations that lack concrete counterparts. Further techniques should be investigated and could most probably be derived based on an implementation and evaluation of the analysis. One such example, as discussed above, is to include a second timeout variable in the analysis. Another example, as also discussed above, is to include a transition counter.

As previously discussed, merging of configurations is not expected to be a usable technique since the configuration contains a lot of concrete information (e.g., the threads’ program counters and the owners of the program locks).

The techniques discussed above (a second timeout combined with a transition counter) should basically guarantee termination of the analysis, provided that suitable limits are chosen. But note that this is still an open question for the analysis presented in this thesis.

## 8.5 Other Applications of the Analysis

Given that the analysis terminates, some interesting results follow. The analysis could be used as a precise deadlock analysis including the timing behavior of the program. If the set of deadlocked configurations (c.f.,  $\tilde{C}^d$  in Algorithm 6.1) is empty, the program is deadlock free up until (and including) the point in time described by the timeout.

Furthermore, the analysis could also be used to determine whether a program is guaranteed to terminate. If the sets containing deadlocked and timed-out configurations (i.e.,  $\tilde{C}^d$  and  $\tilde{C}^t$  in Algorithm 6.1, respectively) are empty, the program is guaranteed to terminate within the returned timing bounds.

## 8.6 Future Work

Some concrete tasks that will be performed in the near future is to implement and evaluate the analysis presented in this thesis. The implementation will be done in a suitable programming language. Which language is yet to be decided, but C/C++ and Erlang are top candidates.

Since PPL is rudimentary and designed to put focus on global data flow and thread synchronization, the implementation could use and analyze a more realistic instruction set. Some candidate instruction sets are LLVM [87], ALF [26, 27], ARM [5] and PowerPC [42]. It could also be possible to make the implementation a flexible framework which could allow the analyzed instruction set to be switched. This could be done by dividing instructions into special classes.

Some model of the underlying architecture (i.e., the function `ABSTIME`) must also be derived. Since the focus of this thesis has excluded any form of definition of `ABSTIME`, some very simple, and perhaps even non-realistic, timing model will most probably be used. Several different timing models should be evaluated to investigate how the characteristics of their definitions affect the complexity of the analysis.

The evaluation will be performed on some suitable benchmark suite of parallel programs. Such a suite is currently being established within the TACLE EU COST Action [86] (a European network of leading researchers within the field of WCET analysis) and will include parallel versions of some of the programs in the Mälardalen WCET Benchmark suite [24]. The benchmark suite should include different types of parallel programs, each of them stressing the analysis in a different way.

It is expected that the evaluation will result in hints pointing to some parts of the analysis that suffer from severe complexity problems. Thus, improvements and strategies for complexity reduction for these parts should be derived and implemented. One point that is already apparent in the case study in Section 7.2 is that the calculations in `DLLOCK`, defined in Algorithm 5.11, should be made tighter if possible (c.f., the result of the Study in Section 7.2, as shown in Table 7.6).

# Bibliography

- [1] S. V. Adve and K. Gharachorloo. Shared memory consistency models: A tutorial. Technical report, Rice University and Western Research Laboratory, 1995.
- [2] R. Alur. Timed automata. In *Lecture Notes in Computer Science*, volume 1633/1999. Springer Berlin / Heidelberg, Jan. 1999.
- [3] R. Alur and D. L. Dill. A theory of timed automata. *Theoretical Computer Science*, 126(2):183 – 235, Apr. 1994.
- [4] A. Andrei, P. Eles, Z. Peng, and J. Rosén. Predictable implementation of real-time applications on multiprocessor systems-on-chip. *International Conference on VLSI Design*, 21:103–110, 2008.
- [5] ARM Ltd. Arm Information Center, 2013. <http://infocenter.arm.com/help/index.jsp>.
- [6] C. Ballabriga, H. Cassé, C. Rochange, and P. Sainrat. OTAWA: An open toolbox for adaptive WCET analysis. In *Software Technologies for Embedded and Ubiquitous Systems*, pages 35–46. Springer, 2011.
- [7] G. Behrmann, A. David, and K. G. Larsen. A tutorial on UPPAAL. In *Proc. 4<sup>th</sup> International School on Formal Methods for the Design of Computer, Communication, and Software Systems*, volume 3185, pages 200–236. Springer Berlin / Heidelberg, Dec. 2004.
- [8] J. Bengtsson and W. Yi. Timed automata: Semantics, algorithms and tools. In *Lecture Notes in Computer Science*, volume 3098/2004, pages 87–124. Springer Berlin / Heidelberg, July 2004.

- [9] A. Burns and A. Wellings. *Real-Time Systems and Programming Languages*. Addison-Wesley, third edition, 2001.
- [10] D. R. Butenhof. *Programming with POSIX Threads*. Addison-Wesley, 1997.
- [11] S. Chattopadhyay, C.-L. Kee, A. Roychoudhury, T. Kelter, P. Marwedel, and H. Falk. A unified WCET analysis framework for multi-core platforms. In *18th IEEE Real-time and Embedded Technology and Applications Symposium (RTAS'12)*, Beijing, China, Apr. 2012.
- [12] A. Colin and G. Bernat. Scope-tree: a program representation for symbolic worst-case execution time analysis. In *Proc. 14th Euromicro Conference on Real-Time Systems, (ECRTS'02)*, pages 50–59, Vienna, June 2002.
- [13] A. Colin and I. Puaut. Worst case execution time analysis for a processor with branch prediction. *Journal of Real-Time Systems*, 18(2/3):249–274, May 2000.
- [14] P. Cousot and R. Cousot. Abstract interpretation: A unified lattice model for static analysis of programs by construction or approximation of fix-points. In *Proc. 4th ACM Symposium on Principles of Programming Languages*, pages 238–252, Los Angeles, Jan. 1977.
- [15] M. B. Dwyer and L. A. Clarke. Data flow analysis for verifying properties of concurrent programs. In *Proc. ACM SIGSOFT '94 Symposium on the Foundations of Software Engineering*, pages 62–75, Dec. 1994.
- [16] J. Engblom. *Processor Pipelines and Static Worst-Case Execution Time Analysis*. PhD thesis, Uppsala University, Dept. of Information Technology, Uppsala, Sweden, Apr. 2002. ISBN 91-554-5228-0.
- [17] A. Ermedahl. *A Modular Tool Architecture for Worst-Case Execution Time Analysis*. PhD thesis, Uppsala University, Dept. of Information Technology, Uppsala University, Sweden, June 2003.
- [18] A. Ermedahl, J. Gustafsson, and B. Lisper. Deriving WCET bounds by abstract execution. In C. Healy, editor, *Proc. 11th International Workshop on Worst-Case Execution Time Analysis (WCET'2011)*, Porto, Portugal, July 2011.

- [19] A. Ermedahl and M. Sjödin. Interval analysis of C-variables using abstract interpretation, 1996.
- [20] C. Ferdinand, R. Heckmann, and B. Franzen. Static memory and timing analysis of embedded systems code. In *3rd European Symposium on Verification and Validation of Software Systems (VVSS'07), Eindhoven, The Netherlands*, number 07-04 in TUE Computer Science Reports, pages 153–163, Mar. 2007.
- [21] D. Grunwald and H. Srinivasan. Data flow equations for explicitly parallel programs. In *Proc. Fourth ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, pages 159–168, 1993.
- [22] N. Guan, M. Stigge, W. Yi, and G. Yu. New response time bounds for fixed priority multiprocessor scheduling. In *Proc. 30<sup>th</sup> IEEE Real-Time Systems Symposium (RTSS'09)*, pages 387–397, Dec. 2009.
- [23] J. Gustafsson. *Analyzing Execution-Time of Object-Oriented Programs Using Abstract Interpretation*. PhD thesis, Dept. of Information Technology, Uppsala University, Sweden, May 2000.
- [24] J. Gustafsson, A. Betts, A. Ermedahl, and B. Lisper. The Mälardalen WCET benchmarks – past, present and future. In B. Lisper, editor, *Proc. 10<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2010)*, pages 137–147, Brussels, Belgium, July 2010. OCG.
- [25] J. Gustafsson and A. Ermedahl. Merging techniques for faster derivation of WCET flow information using abstract execution. In R. Kirner, editor, *Proc. 8<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2008)*, Prague, Czech Republic, July 2008.
- [26] J. Gustafsson, A. Ermedahl, and B. Lisper. ALF (ARTIST2 Language for Flow Analysis) specification. Technical report, Mälardalen University, Västerås, Sweden, Jan. 2009.
- [27] J. Gustafsson, A. Ermedahl, B. Lisper, C. Sandberg, and L. Källberg. ALF – a language for WCET flow analysis. In N. Holsti, editor, *Proc. 9<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2009)*, pages 1–11, Dublin, Ireland, June 2009. OCG.
- [28] J. Gustafsson, A. Ermedahl, C. Sandberg, and B. Lisper. Automatic derivation of loop bounds and infeasible paths for WCET analysis using

- abstract execution. In *Proc. 27<sup>th</sup> IEEE Real-Time Systems Symposium (RTSS'06)*, pages 57–66, Rio de Janeiro, Brazil, Dec. 2006. IEEE Computer Society.
- [29] A. Gustavsson. Worst-case execution time analysis of parallel systems. In *Proc. of Real Time in Sweden 2011 (RTiS2011)*, 2011.
- [30] A. Gustavsson, A. Ermedahl, B. Lisper, and P. Pettersson. Towards WCET analysis of multicore architectures using UPPAAL. In B. Lisper, editor, *Proc. 10<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2010)*, pages 103–113, Brussels, Belgium, July 2010. OCG.
- [31] A. Gustavsson, J. Gustafsson, and B. Lisper. Toward static timing analysis of parallel software. In T. Vardanega, editor, *Proc. 12<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2012)*, volume 23 of *OpenAccess Series in Informatics (OASICs)*, pages 38–47, July 2012.
- [32] A. Gustavsson, J. Gustafsson, and B. Lisper. Toward static timing analysis of parallel systems – technical report. Technical Report 2796, Dept. of Computer Science and Engineering, Mälardalen University, Apr. 2012.
- [33] A. Gustavsson, J. Gustafsson, and B. Lisper. Timing analysis of parallel software using abstract execution. In *Will be submitted to the 15<sup>th</sup> International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI)*, 2014.
- [34] D. Hardy, T. Piquet, and I. Puaut. Using bypass to tighten WCET estimates for multi-core processors with shared instruction caches. In *Proc. 30<sup>th</sup> IEEE Real-Time Systems Symposium (RTSS'09)*, pages 68–77, 2009.
- [35] C. Healy, R. Arnold, F. Müller, D. Whalley, and M. Harmon. Bounding pipeline and instruction cache performance. *IEEE Transactions on Computers*, 48(1):53–70, Jan. 1999.
- [36] C. Healy, M. Sjödin, V. Rustagi, D. Whalley, and R. van Engelen. Supporting timing analysis by automatic bounding of loop iterations. *Journal of Real-Time Systems*, 18(2-3):129–156, May 2000.
- [37] N. Holsti and S. Saarinen. Status of the Bound-T WCET tool. In *Proc. 2<sup>nd</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2002)*, 2002.



- [38] B. Huber and M. Schoeberl. Comparison of implicit path enumeration and model checking based WCET analysis. In *Proc. 9<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2009)*, 2009.
- [39] IEEE and The Open Group. The Open Group Base Specifications Issue 6, 2004. [http://pubs.opengroup.org/onlinepubs/009695399/.functions/pthread\\_spin\\_lock.html](http://pubs.opengroup.org/onlinepubs/009695399/.functions/pthread_spin_lock.html).
- [40] V. Illingworth, editor. *Oxford Dictionary of Computing*. Oxford University Press, fourth edition, 2003.
- [41] Intel Corporation. *Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference*, 1999.
- [42] International Business Machines (IBM) Corporation. *PowerPC User Instruction Set Architecture*, 2005.
- [43] J.-P. Katoen and Friedrich-Alexander. Concepts, algorithms, and tools for model checking. In *Lecture Notes of the Course "Mechanised Validation of Parallel Systems"* (course number 10359) Semester 1998/1999, at Universität Erlangen-Nürnberg.
- [44] T. Kelter, T. Harde, P. Marwedel, and H. Falk. Evaluation of resource arbitration methods for multi-core real-time systems. In C. Maiza, editor, *Proc. 13<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2013)*, pages 1–10. Schloss Dagstuhl, 2013.
- [45] S. C. Kleene. *Introduction to Metamathematics*. North-Holland Publishing Co, Jan. 1980.
- [46] J. Knoop, B. Steffen, and J. Vollmer. Parallelism for free: Efficient and optimal bitvector analyses for parallel programs. *ACM Trans. Program. Lang. Syst.*, 18(3):268–299, May 1996.
- [47] K. G. Larsen, P. Pettersson, and W. Yi. UPPAAL in a nutshell. *International Journal on Software Tools for Technology Transfer (STTT)*, 1(1-2):134–152, Dec. 1997.
- [48] J. Lee, S. P. Midkiff, and D. A. Padua. A constant propagation algorithm for explicitly parallel programs. *International Journal of Parallel Programming*, 26(5):563–589, Oct. 1998.

- [49] X. Li, Y. Liang, T. Mitra, and A. Roychoudhury. Chronos: A timing analyzer for embedded software. *Science of Computer Programming*, 69(1 - 3):56–67, 2007.
- [50] Y.-T. S. Li and S. Malik. Performance analysis of embedded software using implicit path enumeration. In *Proc. ACM SIGPLAN Workshop on Languages, Compilers and Tools for Real-Time Systems (LCT-RTS'95)*, La Jolla, CA, June 1995.
- [51] S. Lim, J. Han, J. Kim, and S. L. Min. A worst case timing analysis technique for multiple-issue machines. In *Proc. 19<sup>th</sup> IEEE Real-Time Systems Symposium (RTSS'98)*, Dec. 1998.
- [52] S.-S. Lim, Y. H. Bae, C. T. Jang, B.-D. Rhee, S. L. Min, C. Y. Park, H. Shin, K. Park, and C. S. Ki. An accurate worst-case timing analysis for RISC processors. *IEEE Transactions on Software Engineering*, 21(7):593–604, Jul 1995.
- [53] B. Lisper. Towards parallel programming models for predictability. In T. Vardanega, editor, *Proc. 12<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2012)*, volume 23 of *OpenAccess Series in Informatics (OASICs)*, pages 48–58, July 2012.
- [54] C. Liu and J. Layland. Scheduling Algorithms for Multiprogramming in a Hard-Real-Time Environment. *Journal of the ACM*, 20(1):46–61, 1973.
- [55] T. Lundqvist. *A WCET Analysis Method for Pipelined Microprocessors with Cache Memories*. PhD thesis, Chalmers University of Technology, Göteborg, Sweden, June 2002.
- [56] T. Lundqvist and P. Stenström. Timing Anomalies in Dynamically Scheduled Microprocessors. Technical Report 99-5, Chalmers University of Technology, Apr 1999.
- [57] M. Lv, N. Guan, W. Yi, Q. Deng, and G. Yu. Efficient instruction cache analysis with model checking. In *Proc. 16<sup>th</sup> IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'10), Work-in-Progress Session*, pages 33–36, Apr. 2010.
- [58] M. Lv, N. Guan, W. Yi, and G. Yu. Combining abstract interpretation with model checking for timing analysis of multicore software. In S. Brandt, editor, *Proc. 31<sup>st</sup> IEEE Real-Time Systems Symposium (RTSS'10)*, pages 339–349, San Diego, CA, Dec. 2010. IEEE.

- 
- [59] MERASA. MERASA project, 2013. <http://www.merasa.org>.
- [60] A. Metzner. Why model checking can improve WCET analysis. In *Lecture Notes in Computer Science*, volume 3114/2004, pages 298–301. Springer Berlin / Heidelberg, July 2004.
- [61] R. Mittermayr and J. Blieberger. Timing analysis of concurrent programs. In *Proc. 12<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2012)*, pages 59–68, 2012.
- [62] F. Nielson, H. R. Nielson, and C. Hankin. *Principles of Program Analysis, 2<sup>nd</sup> edition*. Springer, 2005. ISBN 3-540-65410-0.
- [63] H. R. Nielson and F. Nielson. *Semantics with Applications – A Formal Introduction*. John Wiley & Sons (1992), July 1999.
- [64] OpenMP. OpenMP Application Program Interface, Version 3.0, May 2008. <http://www.openmp.org/mp-documents/spec30.pdf>.
- [65] H. Ozaktas, C. Rochange, and P. Sainrat. Automatic WCET Analysis of Real-Time Parallel Applications. In *Proc. 13<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2013)*. Schloss Dagstuhl–Leibniz-Zentrum fuer Informatik, 2013.
- [66] M. Paolieri, E. Quiñones, F. J. Cazorla, G. Bernat, and M. Valero. Hardware support for WCET analysis of hard real-time multicore systems. In *Proc. 36<sup>th</sup> International Symposium on Computer Architecture (ISCA 2009)*, pages 57–68, 2009.
- [67] M. Paolieri, E. Quiñones, F. J. Cazorla, and M. Valero. GAMC: A generic analyzable memory controller for hard real-time multicore processors. Technical report, Departament d'Arquitectura de Computadors, Universitat Politècnica de Catalunya, May 2009.
- [68] C. Y. Park and A. C. Shaw. Experiments with a program timing tool based on a source-level timing schema. *IEEE Computer*, 24(5):48–57, 1991.
- [69] parMERASA. parMERASA | multi-core execution of parallelised hard real-time applications supporting analysability, 2013. <http://www.parmerasa.eu>.

- [70] D. A. Patterson and J. L. Hennessy. *Computer Organization and Design*. Morgan Kaufmann Publishers Inc., 4<sup>th</sup> edition, Nov. 2008. ISBN 9780123744937.
- [71] D. Potop-Butucaru and I. Puaut. Integrated Worst-Case Execution Time Estimation of Multicore Applications. In *Proc. 13<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2013)*. Schloss Dagstuhl–Leibniz-Zentrum fuer Informatik, 2013.
- [72] A. Prantl, M. Schordan, and J. Knoop. TuBound – a conceptually new tool for worst-case execution time analysis. In R. Kirner, editor, *Proc. 8<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2008)*, pages 141–148, Prague, Czech Republic, July 2008.
- [73] P. P. Puschner and A. Burns. A Review of Worst-Case Execution-Time Analysis. *Real-Time Systems*, 18(2/3):115–128, 2000.
- [74] P. P. Puschner and A. V. Schedl. Computing maximum task execution times – a graph-based approach. *Journal of Real-Time Systems*, 13(1):67–91, July 1997.
- [75] Rapita Systems. Rapitime white paper, 2009. [www.rapitasystems.com/system/files/RapiTime-WhitePaper.pdf](http://www.rapitasystems.com/system/files/RapiTime-WhitePaper.pdf).
- [76] J. Reineke, B. Wachter, S. Thesing, R. Wilhelm, I. Polian, J. Eisinger, and B. Becker. A definition and classification of timing anomalies. In *Proc. 6<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2006)*, July 2006.
- [77] M. Rinard. Analysis of multithreaded programs. In P. Cousot, editor, *Proc. 8th Static Analysis Symposium*, Vol. 2621 of *Lecture Notes in Comput. Sci.*, pages 1–19, Paris, France, July 2001. Springer-Verlag.
- [78] C. Rochange, A. Bonenfant, P. Sainrat, M. Gerdes, J. Wolf, T. Ungerer, Z. Petrov, and F. Mikulu. WCET analysis of a parallel 3D multi-grid solver executed on the MERASA multi-core. In B. Lisper, editor, *Proc. 10<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2010)*, pages 90–100, Brussels, Belgium, July 2010. OCG.
- [79] J. Rosen, A. Andrei, P. Eles, and Z. Peng. Bus access optimization for predictable implementation of real-time applications on multiprocessor systems-on-chip. In *Proc. 28<sup>th</sup> IEEE Real-Time Systems Symposium*

- (*RTSS'07*), pages 49–60, Washington, DC, USA, 2007. IEEE Computer Society.
- [80] J. Schneider and C. Ferdinand. Pipeline behaviour prediction for super-scalar processors by abstract interpretation. In *Proc. ACM SIGPLAN Workshop on Languages, Compilers and Tools for Embedded Systems (LCTES'99)*. ACM Press, May 1999.
- [81] T. Shanley. *x86 Instruction Set Architecture*. Mindshare Press, Dec. 2009.
- [82] A. C. Shaw. Reasoning about time in higher-order software. In *IEEE Transactions on Software Engineering*, volume 15, pages 737–750, 1989.
- [83] F. Stappert and P. Altenbernd. Complete worst-case execution time analysis of straight-line hard real-time programs. *Journal of Systems Architecture*, 46(4):339–355, 2000.
- [84] F. Stappert, A. Ermedahl, and J. Engblom. Efficient longest executable path search for programs with complex flows and pipeline effects. In *Proc. 4<sup>th</sup> International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, (CASES'01)*, Nov. 2001.
- [85] J. Staschulat, S. Schliecker, M. Ivers, and R. Ernst. Analysis of memory latencies in multi-processor systems. In R. Wilhelm, editor, *Proc. 5<sup>th</sup> International Workshop on Worst-Case Execution Time Analysis (WCET'2005)*, Palma de Mallorca, July 2005.
- [86] TACLe. Timing Analysis on the Code Level (TACLe), 2013. <http://www.tacle.eu>.
- [87] The LLVM Project. The LLVM Compiler Infrastructure Project, 2013. <http://llvm.org>.
- [88] S. Thesing. *Safe and Precise WCET Determination by Abstract Interpretation of Pipeline Models*. PhD thesis, Saarland University, 2004.
- [89] UPPAAL. UPPAAL website, 2013. <http://uppaal.org>.
- [90] R. White, F. Müller, C. Healy, D. Whalley, and M. Harmon. Timing Analysis for Data Caches and Set-Associative Caches. In *Proc. 3<sup>rd</sup> IEEE Real-Time Technology and Applications Symposium (RTAS'97)*, pages 192–202, June 1997.

- [91] R. Wilhelm, J. Engblom, A. Ermedahl, N. Holsti, S. Thesing, D. Whalley, G. Bernat, C. Ferdinand, R. Heckmann, T. Mitra, F. Mueller, I. Puaut, P. Puschner, J. Staschulat, and P. Stenström. The worst-case execution time problem — overview of methods and survey of tools. *ACM Transactions on Embedded Computing Systems (TECS)*, 7(3):1–53, 2008.
- [92] Wind River. Wind River VxWorks RTOS, 2013. <http://www.windriver.com/products/vxworks>.
- [93] L. Wu and W. Zhang. Bounding worst-case execution time for multicore processors through model checking. In *Proc. 16<sup>th</sup> IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'10), Work-in-Progress Session*, pages 17–20, Apr. 2010.
- [94] J. Yan and W. Zhang. WCET analysis for multi-core processors with shared L2 instruction caches. In *Proc. 14<sup>th</sup> IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'08)*, pages 80–89, June 2008.
- [95] J. Yan and W. Zhang. Accurately estimating worst-case execution time for multi-core processors with shared direct-mapped instruction caches. In *Proc. 15<sup>th</sup> International Conference on Real-Time Computing Systems and Applications (RTCSA'09)*, pages 455–463, Aug. 2009.

## Appendix A

# Notation & Nomenclature

$exp_1 @ exp_2$	$exp_1$ and $exp_2$ denote the same thing, often a short and a long notation for a configuration.
$b ? exp_1 : exp_2$	If $b$ , then $exp_1$ , otherwise $exp_2$ .
$(o_1, \dots, o_n)$	Ordinary tuple containing $n$ elements.
$\langle o_1, \dots, o_n \rangle$	Special tuple containing $n$ elements. Used to denote complete lattices, Galois connections, configurations, etc.
$[o_1, \dots, o_n]_{e \in \{e_1, \dots, e_m\}}$	Expands to $o_1^1, \dots, o_n^1, \dots, o_1^m, \dots, o_n^m$ ; i.e., one instance of $o_1, \dots, o_n$ for each $e \in \{e_1, \dots, e_m\}$ . Used inside special tuples.
$S$	An arbitrary set (capitalized, italic notation).
$\mathbb{S}$	A standard set (capitalized, blackboard bold notation); e.g., $\mathbb{Z}$ .
<b>Set</b>	A set of analysis-specific elements (first letter capitalized, bold notation); e.g., <b>Thrd</b> .
$\mathcal{P}(S)$	The powerset of $S$ ; i.e., $\{S' \mid S' \subseteq S\}$ .
$S \times S'$	The Cartesian product; i.e., $\{(e, e') \mid e \in S \wedge e' \in S'\}$ .
$\mathcal{P}_{e \in \{e_1, \dots, e_m\}}(exp(e))$	Expands to $exp(e_1) \times \dots \times exp(e_m)$ .

$e, e' \in S$	Short for $e \in S \wedge e' \in S$ .
$\lambda e \in S.exp$	A function from $e$ , which is an element of $S$ , to $exp$ , which is often dependent on the specific $e$ .
$f(s)$	The function $f$ applied on $s$ .
$f \circ g(o)$	Equivalent to $f(g(o))$ .
$f[[o_1]]o_2$	Equivalent to $(f(o_1))(o_2)$ .
$f s$	The function $f$ applied on $s$ . This notation is used when dereferencing mappings.
$\mathbb{f}$	Denotes a state (i.e., a function/mapping from elements to values); e.g., $\mathbb{r}$ .
$\mathbb{f}[s' \mapsto exp]$	Remap; defined as: $\mathbb{f}[s' \mapsto exp] s = \begin{cases} exp & \text{if } s = s' \\ \mathbb{f} s & \text{otherwise} \end{cases}$
ALGFUNC	A function defined in a table or algorithm.
T	One of the threads defined in the analyzed program.
$\Pi$ , <b>Thrd</b>	The analyzed program; i.e., a set of threads.
$r$	Register (thread-local memory).
<b>Reg<sub>T</sub></b>	The set of registers used by thread T.
$x$	Variable (global memory).
<b>Var</b>	The variables defined in the program.
$lck$	Lock (shared resource).
<b>Lck</b>	The locks defined in the program.
$pc$	Program counter (unique for each thread).
$\tilde{f}$	$f$ defined in some abstract domain; i.e., an abstraction of $f$ .
$\mathbb{r}, \tilde{\mathbb{r}}$	Mapping from registers to their values (unique for each thread).
$t^a, \tilde{t}^a$	Accumulated execution time (unique for each thread).
$\mathbb{x}, \tilde{\mathbb{x}}$	Mapping from variables to mappings from threads to their write history for the given variable.



---

$\mathbb{l}, \tilde{\mathbb{l}}$	Mapping from locks to their values.
$c, \tilde{c}$	Configuration (system state).
$\sqsubseteq$	Partial order relation.
$\perp$	The bottom element in a complete lattice.
$\top$	The top element in a complete lattice.
$\sqcup$	The least upper bound operator.
$\sqcap$	The greatest lower bound operator.
$\alpha$	Abstraction function.
$\gamma$	Concretization function.
$\xrightarrow{ax}, \tilde{\xrightarrow{ax}}$	Transition relation for statements (i.e., axioms).
$\xrightarrow{prg}, \tilde{\xrightarrow{prg}}$	Transition relation for threads (i.e., the program).
$t_{to}, \tilde{t}_{to}$	The timeout variable used by the analysis.
$\triangleright$	Begins a comment within algorithms.

**Final configurations** are configurations in which all the threads issue the `halt`-statement.

**Final states** is an alternative notation for final configurations.

**Deadlocked configurations** are configurations that can never reach the final state.

**Timed-out configurations** are configurations that cannot reach the final state before a given point in time, the timeout.

**Truly deadlocked configurations** are abstract configurations that are deadlocked and have valid concrete counterparts; i.e., there is at least one semantically valid concrete configuration that can be abstracted by the given configuration. It must thus be that all threads included in the deadlock are owners of some lock, which has the state *locked*, and are waiting to acquire some other lock, which also has the state *locked*.

**Falsely deadlocked configurations** are abstract configurations that are deadlocked and do not have any valid concrete counterpart; i.e., there is no

semantically valid concrete configuration that can be abstracted by the given configuration. It could thus be that some thread included in the deadlock is the owner of some lock, which has the state *unlocked*, and that some other thread included in the deadlock is waiting to acquire that lock.

**Axiom statements** are labeled statements; i.e., statements that are not composed of several statements.

**Composed statements** are statements that are composed by two or more axiom (i.e., labeled) statements.

**Active statements** are the axiom statements pointed to by the threads' program counters. The active statement is the statement that is executed when the thread is executed. Only one statement in each thread can be active at any given point in time since all the axiom statements within a thread are uniquely labeled.

**Frozen threads** are threads in an abstract configuration whose active statements are lock-statements and the locks they are trying to acquire are currently owned by some other thread.

**Active threads** are not frozen and their active statements are not `halt`. Note that this applies to all threads in any concrete configuration, given that they are not issuing the `halt`-statement, since only threads in an abstract configuration can be frozen.

**Executing threads** are the active threads that will execute their active statement at the nearest point in time.

**BCET** (Best-Case Execution Time) is the shortest possible execution time of the program, given a certain set of initial states.

**WCET** (Worst-Case Execution Time) is the longest possible execution time of the program, given a certain set of initial states.

## Appendix B

# List of Assumptions

4.1	TIME is non-negative . . . . .	47
4.3	TIME is non-zero when spin-locking . . . . .	47
5.50	ABSTIME is safe and non-negative . . . . .	89



## Appendix C

### List of Definitions

3.1	Monotone function . . . . .	16
3.2	Completely additive function . . . . .	16
3.3	Completely multiplicative function . . . . .	17
3.9	Galois connection . . . . .	20
3.10	Galois insertion . . . . .	20
3.11	Induced function . . . . .	21
3.12	Adjunction . . . . .	21
3.26	Partial order . . . . .	32
3.27	Greatest lower bound . . . . .	32
3.28	Least upper bound . . . . .	32
3.29	Abstraction function, $\alpha$ . . . . .	32
3.30	Alternative definition – Concretization function, $\gamma$ . . . . .	32
3.31	Interval . . . . .	33
3.32	concretization of intervals . . . . .	33
3.33	Partial order for intervals . . . . .	33
3.34	Greatest lower bound for intervals . . . . .	33
3.35	Least upper bound for intervals . . . . .	34
3.36	Abstraction to interval . . . . .	34
4.4	Valid concrete configuration . . . . .	50
4.7	Collecting semantics . . . . .	52
5.1	Concretization of an abstract register state . . . . .	54
5.2	Partial order for abstract register states . . . . .	54

5.3	Greatest lower bound of abstract register states . . . . .	54
5.4	Least upper bound of abstract register states . . . . .	56
5.5	Abstraction of a set of register states . . . . .	56
5.7	Boolean restriction . . . . .	57
5.8	Concretization of an abstract variable state . . . . .	58
5.9	Abstraction of a set of variable states . . . . .	58
5.11	Partial order of writes, $\hat{\sqsubseteq}_w$ . . . . .	60
5.12	Least upper bound of writes, $\hat{\sqcup}_w$ . . . . .	60
5.13	Time precedence, $\hat{<}_t$ . . . . .	60
5.14	Partial order for abstract variable states . . . . .	61
5.15	Greatest lower bound of abstract variable states . . . . .	61
5.16	Least upper bound of abstract variable states . . . . .	61
5.17	Time of most recent write . . . . .	61
5.18	Safe write history . . . . .	62
5.19	Safe value of $x$ as seen by thread $T$ . . . . .	62
5.20	Safe partial order of abstract variable states . . . . .	65
5.21	Safe lower bound of abstract variable states . . . . .	65
5.22	Safe upper bound of abstract variable states . . . . .	65
5.28	Concretization of an abstract lock state . . . . .	74
5.29	Abstraction of a set of lock states . . . . .	74
5.30	Partial order of abstract lock states . . . . .	76
5.31	Greatest lower bound of abstract lock states . . . . .	76
5.32	Least upper bound of abstract lock states . . . . .	76
5.35	Concretization of an abstract configuration . . . . .	79
5.36	Partial ordering of two abstract configurations . . . . .	79
5.38	Greatest lower bound for two abstract configurations . . . . .	80
5.39	Least upper bound for two abstract configurations . . . . .	80
5.40	Abstraction of a set of configurations . . . . .	81
5.42	Abstraction of a set of axiom input configurations . . . . .	83
5.43	Concretization of an abstract axiom input configuration . . . . .	83
5.44	Abstraction of a set of axiom output configurations . . . . .	83
5.45	Concretization of an abstract axiom output configuration . . . . .	83
5.48	Soundness of the abstract axiom transition relation . . . . .	85
6.9	BCET and WCET . . . . .	158

## Appendix D

### List of Figures

4.6	Illustration of how $\mathbf{Thrd}_{exe}$ is determined. . . . .	46
5.3	The time-stamps of the writes considered by READ. . . . .	68
5.7	Abstract lock state transitions. . . . .	132
6.1	Timeout for recursion in ABSEXE. . . . .	151
7.4	Communicating threads – Configuration relations. . . . .	165
7.7	Synchronization (Deadlock) – Configuration relations. . . . .	168
7.10	Synchronization (Deadline miss) – Configuration relations. . . . .	170
8.1	Lock owner assignments based on $\tilde{c} \in \mathbf{C\tilde{o}nf}$ resulting in one valid and one invalid configuration. . . . .	174
8.2	Lock owner assignments based on $\tilde{c} \in \mathbf{C\tilde{o}nf}$ resulting in two valid and two invalid (i.e., falsely deadlocked) configurations. . . . .	175





# Appendix E

## List of Tables

4.1	The Syntax of PPL. . . . .	38
4.2	Semantics of concrete axiom transitions. . . . .	42
4.3	Semantics of concrete program transitions. . . . .	43
4.4	Definition of STM and LABELS. . . . .	44
4.5	Definition of STT, OWN, DL, POWN and REL. . . . .	45
4.7	Semantics of concrete evaluation of arithmetic expressions. . . . .	48
4.8	Semantics of concrete evaluation of boolean expressions. . . . .	48
5.1	PPL operators defined for interval arguments. . . . .	55
5.2	The abstract function evaluating arithmetic expressions. . . . .	57
5.4	Definition of $S\tilde{T}T$ , $O\tilde{W}N$ , $D\tilde{L}$ , $PO\tilde{W}N$ and $RE\tilde{L}$ . . . . .	75
5.5	Semantics of abstract axiom transitions. . . . .	84
5.6	Semantics of abstract program transitions. . . . .	88
7.1	Communicating threads – Program. . . . .	161
7.2	Communicating threads – Configurations (First half). . . . .	163
7.3	Communicating threads – Configurations (Second half). . . . .	164
7.5	Synchronization (Deadlock) – Program. . . . .	166
7.6	Synchronization (Deadlock) – Configurations. . . . .	167
7.8	Synchronization (Deadline miss) – Program. . . . .	169
7.9	Synchronization (Deadline miss) – Configurations. . . . .	170



## Appendix F

### List of Algorithms

5.1	Partial Order of Abstract Variable States . . . . .	63
5.2	Earliest Write for a Thread . . . . .	64
5.3	Meeting Two Abstract Variable States . . . . .	66
5.4	Joining Two Abstract Variable States . . . . .	67
5.5	Write to Variable . . . . .	68
5.6	Read from Variable . . . . .	69
5.7	Time of Most Recent Write . . . . .	69
5.8	Time of Most Recent Write in Thread . . . . .	69
5.9	Trim Variable State . . . . .	72
5.10	Split Set of Writes . . . . .	72
5.11	Determine Deadline for Lock Owner Assignment . . . . .	90
5.12	Determine Accumulated Execution Time . . . . .	90
5.12	<i>Cont.</i> Determine Accumulated Execution Time . . . . .	91
6.1	Abstract Execution . . . . .	138
6.2	Choose an Element . . . . .	139
6.3	Final Abstract Configuration . . . . .	139
6.4	Deadlocked Abstract Configuration . . . . .	140
6.5	Timed-Out Abstract Configuration . . . . .	140
6.6	Valid Abstract Configuration . . . . .	140
6.7	Determine if Graph Has Cycles . . . . .	141
6.8	Threads Executing a Possibly Unsafe Load Statement . . . . .	141
6.9	Global Variables in an Abstract Configuration . . . . .	142

**202    Appendix F. List of Algorithms**

---

6.10	Threads to Execute in Abstract Configuration . . . . .	142
6.11	Get Variable in Load Statement . . . . .	142
6.12	Get Register in Load Statement . . . . .	142
6.13	BCET/WCET Analysis . . . . .	157

# Appendix G

## List of Lemmas

3.4	Completely multiplicative functions . . . . .	17
3.14	Relation between $\alpha$ and $\gamma$ . . . . .	22
3.15	Galois connection – Existence . . . . .	23
3.18	Monotonicity of $\alpha_{\emptyset}$ . . . . .	25
3.19	Monotonicity of $\gamma_{\emptyset}$ . . . . .	26
3.23	Monotonicity of $\gamma_s$ . . . . .	28
3.37	Monotonicity of $\gamma_{int}$ . . . . .	34
3.38	Monotonicity of $\alpha_{int}$ . . . . .	34
4.2	Time only moves forward . . . . .	47
4.5	$\xrightarrow{prg}$ preserves lock state validity . . . . .	50
4.6	Properties of $\mathbb{1}''$ . . . . .	51
5.23	Soundness of WRITE . . . . .	68
5.24	Soundness of MOSTRECENTWRITETIMETHREAD . . . . .	70
5.25	Soundness of MOSTRECENTWRITETIME . . . . .	70
5.26	Soundness of READ . . . . .	70
5.27	Soundness of TRIM . . . . .	71
5.33	Monotonicity of $\gamma_{lock}$ . . . . .	77
5.37	Monotonicity of $\gamma_{conf}$ . . . . .	79
5.49	Soundness of $\xrightarrow{ax}$ . . . . .	85
5.51	Time accumulation . . . . .	94
5.52	Thread isolation . . . . .	94

5.53	Soundness of DLLOCK . . . . .	95
5.54	Partial soundness of ACCTIME . . . . .	100
5.55	Properties of owner assignment for lock-transitions . . . . .	104
5.56	Soundness of $\xrightarrow[\text{prg}]{\sim}$ , no frozen thread . . . . .	108
5.57	Soundness of $\xrightarrow[\text{prg}]{\sim}$ , frozen thread . . . . .	119
5.58	Soundness of $\xrightarrow[\text{prg}]{\sim}$ , final state . . . . .	130
6.1	Soundness of CYCLE . . . . .	141
6.2	Soundness of EXETHRD . . . . .	143
6.3	Soundness of GLOBALVAR . . . . .	144
6.4	Soundness of EXELOADTHRD . . . . .	144
6.5	Soundness of ISDEADLOCK . . . . .	145
6.6	Soundness of ISTIMEOUT . . . . .	145
6.7	Soundness of ISVALID . . . . .	146
6.8	Soundness of ABSEXE . . . . .	148
6.10	Soundness of ANALYSIS . . . . .	158

# Appendix H

## List of Theorems

3.5	Complete lattice – Lifting . . . . .	18
3.6	Complete lattice – Cartesian product . . . . .	18
3.7	Complete lattice – Total function space . . . . .	19
3.8	Complete lattice – Monotone function space . . . . .	19
3.13	Adjunctions and Galois connections . . . . .	21
3.16	Galois connection – Independent attribute method . . . . .	24
3.17	Galois connection – Lifted independent attribute method . . . . .	24
3.20	Galois connection – Double lifting . . . . .	26
3.21	<i>Not</i> a Galois connection – Double lifting . . . . .	27
3.22	Galois connection – Function space . . . . .	28
3.24	Galois connection – Lifted function space . . . . .	29
3.25	Galois connection – Indexing . . . . .	30
3.39	Galois insertion – Intervals . . . . .	35
5.6	Galois connection – Register states . . . . .	56
5.10	Galois connection – Variable states . . . . .	59
5.34	Galois connection – Lock states . . . . .	77
5.41	Galois connection – Configurations . . . . .	81
5.46	Galois connection – Axiom input configurations . . . . .	83
5.47	Galois connection – Axiom output configurations . . . . .	83





# Index

- NOTE, 15, 37, 39, 53, 54, 60, 62, 65, 100, 137, 156
- abstract domain, 6, 20
- abstract execution, 6–9, 12
- abstract interpretation, 6, 7, 11, 13, 15, 39, 176
- abstraction, 6, 7, 9, 20, 48, 53, 56, 137, 171, 173, 190
- anti-symmetric relation, *see* relation
- BCET, *BCET*, 3, 4, 6–9, 12, 157–159, 162, 168, 169, 192
- Best-Case Execution Time, *see* BCET, *BCET*
- bottom element, 16
- bounds
  - lower, 16
  - greatest, 16
  - upper, 16
  - least, 16
- calculation, 4
- completely additive function, *see* function
- completely multiplicative function, *see* function
- concrete domain, 20
- COST Action, 178
- dynamic analysis, 4
- embedded system, 1
- estimation
  - safe, 3, 4
  - tight, 4
- fixed-point calculation, 92
- flow analysis, 4
- function
  - completely additive, 16
  - completely multiplicative, 16
  - monotone, 16
  - partial, 16
  - total, 16
- global memory, *see* variable
- greatest lower bound, *see* bounds
- halting-problem, 5
- least upper bound, *see* bounds
- local memory, *see* register
- lock, 37
- low-level analysis, 4
- lower bound, *see* bounds
- Mälardalen WCET Benchmark suite, 178
- model-checking, 1, 5, 6, 12, 13
- monotone function, *see* function
- multi-core CPU, 2, 3, 7, 12–14, 37, 53, 171

- partial function, *see* function
- partial ordering, 16
- real-time system, 1–3, 5–7
  - hard, 2, 3
  - soft, 2
- reflexive relation, *see* relation
- register, 37
- relation, 15
  - anti-symmetric, 16
  - reflexive, 16
  - transitive, 16
- safe estimation, *see* estimation
- shared memory, 2–4, 7, 13, 14, 37, 172, 176
- single-core CPU, 5, 14
- static analysis, 4
- TACLe, *see* COST Action
- tight estimation, *see* estimation, 7
- top element, 16
- total function, *see* function
- transitive relation, *see* relation
- UPPAAL, 6, 12
- upper bound, *see* bounds
- variable, 37
- WCET, *WCET*, 3–9, 11–14, 157–159, 162, 168, 169, 178, 192
- Worst-Case Execution Time, *see* WCET, *WCET*



